3D Nanofabrication of Fluidic Components by Corner Lithography

Narges Burouni

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3D NANOFABRICATION OF FLUIDIC COMPONENTS BY CORNER LITHOGRAPHY

DISSERTATION

to obtain
the degree of doctor at the University of Twente,
on the authority of the rector magnificus,
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on account of the decision of the graduation committee,
to be publicly defended
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by

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in Tehran, Iran

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To My Grandfather and to My Love Hamidreza

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Abstract

A reproducible wafer-scale method to obtain 3D nanostructures using a low-budget lithography tool is investigated. This method, called corner lithography, explores the conformal deposition and the subsequent timed isotropic etching of a thin film in a 3D shaped silicon template. Moreover, it offers sub-micron lithography in wafer scales that allows wide range of miniaturization of nano devices, which are uniform and compatible with geometrical expectation. The technique leaves a residue of the thin film in sharp concave corners, which can be used as structural material or as an inversion mask in subsequent steps. Corner lithography is demonstrated based on a theoretical foundation including a statistical analysis that enables the construction of wires, slits and dots into versatile three-dimensional structures. The potential of corner lithography is studied by fabrication of functional 3D components, in particular i) novel tips containing nano-apertures at or near the apex for AFM-based liquid deposition devices, ii) novel 3D nanowire pyramid as scanning probe for atomic force microscopy, and iii) a novel particle or cell trapping device using an array of nanowire frames. The use of these arrays of nanowire cages for capturing single primary bovine chondrocytes by a droplet seeding method is successfully demonstrated, and changes in phenotype are observed over time, while retaining them in a well-defined pattern and 3D microenvironment in a flat array.
Moreover, an innovative method that is called "repeated corner lithography" is introduced which gives higher resolution and employs to obtain sub-30 nm apertures and pyramidal nanowires, while maintaining the mechanical stability of the micron structures.

Keywords: Wafer-scale Fabrication, Nanoaperture, Corner Lithography, 3D Nanofabrication, Fluidic Components, Cell-trapping Device, Pyramidal Nanowire, Atomic Force Microscopy, Repeated Corner Lithography, Self Aligned Sub-30 nm Apertures.

Samenvatting

Een reproduceerbare waferschaal-methode om 3D-nanostructuren te verkrijgen is onderzocht gebruikmakende van een goedkope lithografische methode. Deze methode, genaamd hoeklithografie, verkent de conforme depositie en het daaropvolgende, tijdbepaalde isotrope-etsen van een dunne film in een 3D-gevormde siliciummal en biedt waferschaal sub-micron lithografie met de mogelijkheid tot een groot bereik in miniaturisatie van nanodevices, welke uniform en compatible zijn met geometrische verwachtingen. De techniek behoudt een residue van de dunne film in scherpe concave hoeken, welke gebruikt kan worden als structurerend materiaal of als inversiemasker in vervolgstappen. Hoeklithografie wordt aangetoond - gebaseerd op een theoretische basis inclusief een statistische analyse welke de constructie van draden, sleuven en punten toelaat tot vorming van veelzijdige drie-dimensionale structuren. De potentie van hoeklithografie is bestudeerd door fabricage van functionele 3D-componenten, in het bijzonder i) nieuwe tips met nano-openingen op of dichtbij de spits, voor AFM-gebaseerde vloeistof-depositie- devices, ii) nieuwe 3D-nanodraadpyramide als aftastsonde voor atomic-force microscopie en iii) een nieuwe deeltjes of cel-trapping device gebruikmakende van een matrix van nanodraadgeraamtes. Het nut van deze matrices van nanodraadgeraamtes voor het vangen van enkele primaire bovine chondrocytes door een druppel-kiem methode is sucessvol gedemonstreerd en veranderingen van het phenotype zijn gedurende de tijd geobserveerd, terwijl ze vastgehouden worden in een goed gedefineerd patroon en 3D-micro-omgeving in een platte matrix. Bovendien, een innovatieve methode genoemd "herhaalde hoek- lithografie" wordt geintroduceerd welke hogere resolutie geeft, toegepast om sub-30nm aperatures en pyramidische nanodraden te maken, met behoud van mechanische stabiliteit van de micron-structuren.

Trefwoorden: Waferschaal fabricage, Nano-openingen, Hoeklithografie, 3D-nanofabricage, Fluidische componenten, Cell-trapping device, Pyramidische nanodraden, Atomic-force microscopie, Herhaalde hoeklithografie, Zelf-uitricht sub-30 nm openingen.

Acknowledgments

One of the journeys in my life has been finished. When I look over the journey and remember all the experiences, successes, challenges, people, friends and family who have helped and supported along, I realize how much I have learned and gained. Such a valuable journey!

One of my hobbies is oil painting. I spent a lot of time with my grandfather (baba jooni) in the past and had many lovely conversations with him about several topics, while I was painting. He was a good painter and creative architect and more importantly good leader at his job. He was living alone after my grandmother passed away and was coming to our house twice a week. I was eagerly waiting for those days to talk with him and do painting together. Many people loved him because of his positive and encouraging spirit and kind behavior. I always talked about all of my dreams with him, and one of those was doing my PhD.

I still remember, after my master thesis defence at Sharif University of Technology, when the committee members came out of the room and announced the decision, all my friends and family members came for congratulating me, I saw him standing in the corner and looking at me with a beautiful smile and a bunch of violet flowers in his hands. He slowly came to me (he was 72 years old) and said: *”Congratulations, now you can start ... I hope to see your PhD ceremony as well ...”* Few months later, when I was in the middle of painting a big canvas, I came to the Netherlands to start my PhD at University of Twente, Faculty of Electrical Engineering, Mathematics and Computer Science (EEMC), within the Transducer Science and Technology Group (TST). I left him, my canvas, my job at the company, my students, my family and friends to start a new journey in my life.

PhD is not only a 4-years research project, but it is a large package including a lot of exciting and learning experiences. You may lead different projects before or after the doctoral time, but PhD is different and unique. Now, it is the end of my PhD and I am very proud and happy about this project and its achievements.

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My beloved grandfather passed away some months after I started my PhD. This thesis is dedicated to all the people who never give up following their dreams ...

List of papers

This thesis is based on work reported in the following papers, referred to by Roman numerals in the text.

Journal Papers

I J.W. Berenschot, N. Burouni, B. Schurink, J.W. van Honschoten[1], R. Sanders, R. Truckenmüller, H.V. Jansen, M. Elwenspoek, A. van Apeldoorn and N.R. Tas, 3D Nanofabrication of Fluidic Components by Corner Lithography, Small 8 3823-31
DOI:10.1002/smll.201201446
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II N. Burouni, E. Berenschot, M. Elwenspoek, E. Sarajlic, P. Leussink, H. Jansen and N.R. Tas, Wafer-scale Fabrication of Nanoapertures Using Corner Lithography, Nanotechnology 24 285303
DOI:10.1088/0957-4484/24/28/285303

III N. Burouni, J.W. Berenschot, M. Elwenspoek and N.R. Tas, 3D Nanofabrication of Self Aligned Sub-30 nm Aperture and Nanowires by Repeated Corner Lithography, (to be submitted).

[1]Dr. Joost W. van Honschoten is deceased, as of January 12th, 2011.

Conference Papers

I N. Burouni, J.W. Berenschot, M. Elwenspoek and N.R. Tas, *Dimensional Control in Corner Lithography for Wafer Scale Fabrication of Nano Aperture*, Oral Presentation, In Proc. IEEE NEMS Conference, Kaohsiung, Taiwan, February 20-23, 2011.

II N. Burouni, E. Sarajlic, M. Siekman, L. Abelmann and N. Tas, *A Scanning Microscopy Probe with Pyramidal Nanowire Tip For Both Thermal and Magnetic Imaging*, Oral Presentation, $MESA^+$ Micro and Nano Fluidics Day, 21 July 2011.

III N. Burouni, E. Sarajlic, M. Siekman, L. Abelmann and N. Tas, *Pyramidal Nanowire Tip for Atomic Force Microscopy and Thermal Imaging*, Oral Presentation, In Proc. IEEE NEMS 2012, Kyoto, Japan.

IV N. Burouni, J.W. Berenschot, M. Elwenspoek and N.R. Tas, *3D Nanofabrication of Components by Repeated Corner Lithography: Self Aligned Sub 50-nm Aperture*, Oral Presentation, IEEE NANO Conference, Birmingham, UK, August 20-23, 2012 (Invited Paper, Chairman).

V J.W. Berenschot, N. Burouni, B. Schurink, J.W. van Honschoten, R. Sanders, R. Truckenmüller, H.V. Jansen, M. Elwenspoek, A. van Apeldoorn and N.R. Tas, *3D Nanofabrication of Fluidic Components by Corner Lithography*, Oral Presentation, Annual $MESA^+$ Meeting, 18 September 2012 (Invited Speaker).

VI J.W.Berenschot, N. Burouni, E. Sarajlic, H.V. Jansen, A.A. van Apeldoorn, N.R. Tas, *3D Fabrication of Micro- and Nanostructures by Corner Lithography*, Poster Presentation, MMB April 2013.

VII J.W.Berenschot, N. Burouni, E. Sarajlic, N.R. Tas, *Corner Lithography as a Versatile 3D Nanofabrication Technique*, Invited Presentation, ICSS December 2013.

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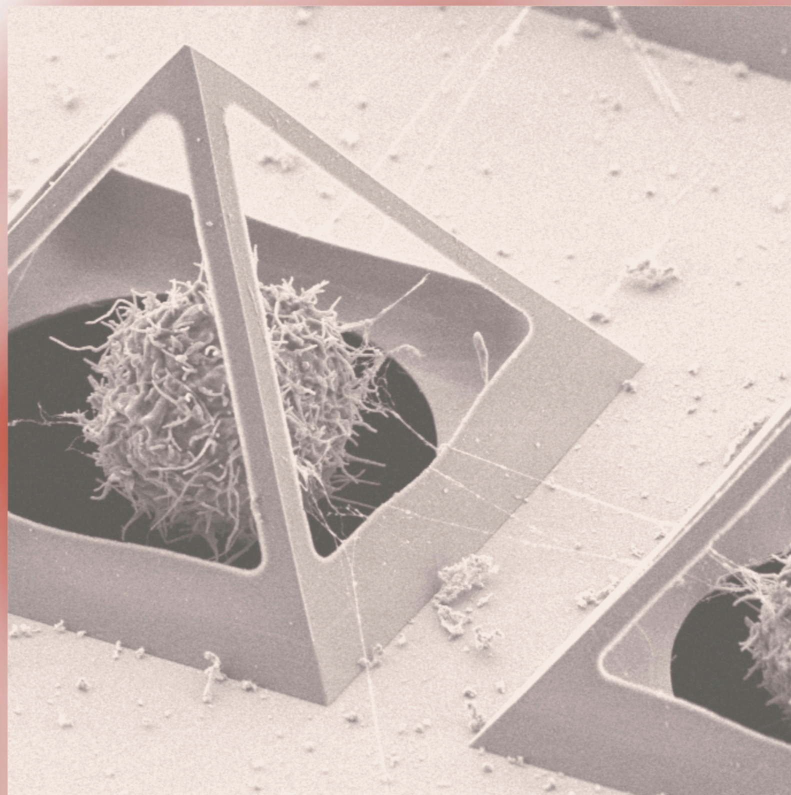

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3D Nanofabrication of Fluidic Components by Corner Lithography

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Abbreviations and Acronyms

AFM	Atomic Force Microscopy
DEP	Di-electrophoretic
DPL	Dip Pen Lithography
DPN	Dip Pen Nanolithography
ECM	Extra Cellular Matrix
ESEM	Environmental Scanning Electron Microscope
FIB	Focus Ion Beam
FPL	Fountain Pen Lithography
LOCOS	LOCal Oxidation of the Silicon
LPCVD	Low Pressure Chemical Vapor Deposition
MEMS	Micro Electro Mechanical Systems
NADIS	Nano-Scale Dispensing
NEMS	Nano Electro Mechanical Systems
NFP	Nano Fountain Pen
NSOM	Near-field Scanning Optical Microscopy
RH	Relative Humidity
RIE	Reactive Ion Etching
SD	Standard Deviation
SEM	Scanning Electron Microscopy
SHPM	Scanning Hall Probe Microscopy
SICM	Scanning Ion-Conductance Microscopy
SThM	Scanning Thermal Microscopy
STM	Scanning Tunneling Microscopes

Part I

Scientific chapters

Chapter 1

Introduction

Nanotechnology and its applications have grown rapidly in the past ten years. This rapid growth is largely due to the very quick advances in nanofabrication techniques employed to fabricate nano-devices. Up to now, there is a rising interest in miniaturization of devices and systems in industries and scientific domains. The advantages of producing smaller systems and devices are various, including lower costs, lower power consumption and higher performance. Nanostructures are manufactured using a number of different techniques depending upon which best fits the intended application and hence, the fabrication and integration of nanostructures into devices strongly depends on the capabilities and limitations of the current manufacturing technologies.

Despite the ability to manufacture nanostructures with varying degrees of complexity, two fundamental trade-offs exists for all current nanofabrication technologies that limit the types of nanostructures that can be manufactured. The first and most inhibiting limitation is that complex three-dimensional (3D) shapes with controlled features are difficult to make. The second limitation is that, as feature sizes shrink into the nano-domain, it becomes increasingly difficult to accurately maintain those features over large depths and heights; features can be created with either high control or complexity but low aspect-ratios.

These trade-offs limit the use and study of many nanotechnologies such as nano-imprint lithography, metamaterials, photonic crystals, and nanofluidics where complex, high aspect-ratios features are needed to improve device performance and efficiency (Boltasseva et al., 2008). As such, new technologies are needed that can controllably create both two-dimensional (2D) and 3D nanostructures with high complexity, high aspect-ratios, and at relatively low costs.

1.1 3D Nanofabrication Methods - Overview, Benefits and Limitations

Several methods have been developed in the microelectronics industry, which are appropriate for patterning 2D structures on ultra-flat glass or semiconductor surfaces. The repetitive patterning of 2D structures has been used to indirectly fabricate 3D structures on a single substrate, which is difficult to implement for multi-layer structures and requires sophisticated facilities. Several research groups have been also interested in developing alternative methods to this technique (Loo et al., 2002b,a; Zaumseil et al., 2003; Menard et al., 2004; Jeon et al., 2004).

Furthermore, some methods are based on electron beam lithography (EBL) (Yamazaki et al., 2004), nano-imprint lithography (NIL) (Austin et al., 2004), deep reactive ion etching (DRIE) (Morton et al., 2008), multi-directional (or multiangled) etching (Takahashi et al., 2009), proton beam writing (van Kan et al., 2006), wafer bonding (Noda et al., 2000), colloidal sedimentation (Velev et al., 1997; Johnson et al., 1999; Vlasov et al., 2001), polymer phase separation (Fink et al., 1999; Bates, 1991; Park et al., 1997; Böltau et al., 1998; Morkved et al., 1994), templated growth (Yang et al., 1997; Martin, 1995; Hoyer, 1996; Jacobs et al., 2002), fluidic assembly (Jacobs et al., 2002; Yeh and Smith, 1994; Bowden et al., 2001), interference lithography (Campbell et al., 2000; Divliansky et al., 2003), writing, embossing and other methods (Xia et al., 1999; Mirkin and Rogers, 2001; Smay et al., 2002). These methods have their own benefits and limitations. It is of greatest importance to create and assemble individual nanometer-scale components in a controllable manner to produce useful materials, devices and systems.

One proposed method for 3D fabrication of nanostructures is called self-assembly (Glotzer, 2004), in which the ordering and assembly of structures at feature sizes of a few nanometers are left to the materials. In this method, the energy is minimized and structures are typically periodic and closely packed. Self-assembly benefiting from bottom-up synthetic chemistry has provided an effective approach of producing materials and organizing them into functional nanotechnology structures that are designed for specific purposes. One of the limitations of self-assembly method is that it is difficult to reach perfect ordering by self-assembly. The most fundamental disadvantage of self-assembly is due to the fact that for every product, the structure of the parts must encode the structure of the whole. This requires that components should be more complex, which tends to make design and fabrication more difficult.

Nanostructures can be fabricated with very precise 3D patterning by

origami method (Gracias, 2013). The nanostructured origami process provides several advantages. First, a multi-layer device can be made by patterning and repeatedly folding a single layer. Because only one layer needs to be patterned, fabrication difficulties associated with multi-layer devices can be avoided. Improved alignment and spacing among the folded layers can be achieved through the use of pyramid-shaped alignment features (In et al., 2005). In addition, whereas current nanofabrication methods are largely limited to building nanostructures on the top surface of a horizontally oriented substrate, the origami method allows the pattern surfaces to be oriented arbitrarily within the final 3D system. The approaches that are inspired from origami are very important at the nanoscale wafer-scale fabrication. Mechanized folding becomes more difficult to fabricate smaller micro- and nanoscales. At scaled down sizes, hands-free mechanisms are needed to generate the torques that are required to lift segments of the sheet out of plane (Syms et al., 2003; Leong et al., 2010; Cho et al., 2011).

Carbon nanotubes are fabricated by various methods that include laser ablation, arc-discharge, catalic chemical vapor deposition (CVD) and more (Cabrini and Kawata, 2012). Depending on the methods, the grown nanotubes are single-wall carbon nanotubes (SWCNTs), multi-wall carbon nanotubes (MWCNTs), or sometimes double-walled carbon nanotubes (DWCNTs). At the moment, it is almost possible to selectively grow SWCNTs and MWCNTs, but it is very difficult to selectively grow SWCNTs with a specific chirality (grapheme sheet). The carbon nanotube is a very interesting material because it has a very small diameter. For the SWCNT, it is about 1 nm, which is not possible to realize with conventional lithography techniques. Therefore, it is a natural choice for the study of the low-dimensional electron transport (Cabrini et al., 2012).

Holographic lithography (Campbell et al., 2000) is one example of such category that is well suited to the production of 3D structures with submicrometer periodicity. This technique is able to make microperiodic polymeric structures to be used as templates to create complementary structures with higher refractive-index contrast. Compared with other fabrication methods, the holographic lithography method possesses many remarkable advantages such as high resolution, low cost, and easy-to-construct various lattice structures (Toader et al., 2004). However, there may also exist remarkable disadvantage: pre-designed structural defects are difficult to introduce in 3D photonic crystals fabricated by the holographic lithography method (Gong and Hu, 2014).

Direct laser writing based on multi-photon absorption can be mentioned as one of the most developed methods that can rapidly fabricate prototypes with desired shapes. Direct laser writing has been employed by Deubel et al.

(2004) for 3D nanofabrication photonic-crystal templates for telecommunications. It was found that direct laser writing by multi-photon polymerization of a photoresist could be used as a technique for rapid, cheap and flexible fabrication of nanostructures for photonics. Ledermann et al. (2006) has investigated the use of direct laser writing combined with a silicon inversion procedure to achieve high-quality silicon inverse icosahedral structures.

In another versatile method that is called inkjet printing, small amounts of liquids can be delivered. This method is suitable for fabrication of DNA microarrays (Okamoto et al., 2000) and depositing self-assembled monolayers (SAMs) or proteins (Pardo et al., 2003). The uniformity of SAMs and DNA layers that are deposited by inkjet method has been investigated using a selective etch method by Bietsch et al. (2004). Printing of functional electronic devices has also been performed using inkjet deposition of polymers (Sirringhaus et al., 2000). However, the current printing technologies have constrains due to limitation of the ink viscosity, clogging of small size nozzles, and generation of pattern smaller than the nozzle size (Le, 1998).

In addition, the ability to stack and bond strained silicon nanomembranes (SiNMs) provides an interesting platform to study the effects of interacting surfaces and interfaces. It is well known from wafer bonding experiments that bonding of two silicon wafers at a misfit angle produces a periodic network of dislocations. By using membranes, the thickness of the bonded layer (membrane) can be varied, and hence, the degree of strain propagation to the surface (Kiefer et al., 2007). More recently, membrane stacking has been used as an alternative for layer-by-layer processes to fabricate 3D structures. It has provided higher yield and quicker turnaround time. Membranes are fabricated in silicon nitride with free-standing photonic-structures. However, major issues can be addressed as removing dust particles from membranes, cleanly cutting membranes away from their frame, and avoiding any lateral shifting when membranes are brought into contact (England et al., 2012; Patel and Smith, 2007).

This thesis details a new nanofabrication technique developed to overcome some of the limitations discussed in the previous paragraphs. In view of the large number of challenges in fabricating the types of 3D nanostructures that are important for many areas of nanotechnology, we introduce "corner lithography" and an innovative method that is called "repeated corner lithography" in wafer-scale 3D nanofabrication era. It is a general nanofabrication technique that is capable of producing a variety of well-ordered 3D nanostructures with several applications. However, this method needs sharp corners to fabricate small 3D structures. This approach could be used in a wide range of micro-electromechanical systems applications that require the fabrication of tips or pyramidal pits. Finally, in this thesis we

show that corner lithography is a reproducible, well controlled, and uniform method in wafer-scale and materials. It will be described in greater details in the upcoming chapters that corner lithography method can be employed to fabricate wafer-scale nanoapertures. Furthermore, 3D nanofabrication of fluidic components by corner lithography will be discussed. Efforts have been focused on the controllability and accuracy of the corner lithography method to design a reliable wafer-scale technique.

1.2 Aim of Thesis

The main aim of this thesis was to develop a new three-dimensional nanofabrication method that can be employed to fabricate patterns in wafer-scale, which is quick, low cost with high resolution and accuracy. This main aim is broken down to several sub projects:

- To investigate the sensitivity and resolution of corner lithography method for different fabrication process steps and show its high accuracy and uniformity, reproducibility, wafer-scale productivity and very well size control in 3D nanofabrication process.
- To demonstrate very fascinating 3D nanostructures that can be fabricated by corner lithography in the batch-wise fabrication of sub-micron features (apertures and wires) and their integration into functional fluidic devices.
- To design and fabricate a novel wireframe probe for atomic force using corner lithography that can be applied in scanning thermal microscopy, to either measure the thermal conductance or temperature of surfaces.
- To investigate a novel method that is called ”repeated corner lithography” to produce sub-30 nm nanoapertures and pyramidal nanowire frames in three-dimensions that can offer more mechanical stabilities in the structures.

1.3 Thesis Outline

Chapter 2 describes the wafer-scale fabrication of nanoapertures using corner lithography method and explains the control of the size of the aperture with diameter less than 50 nm using a low-budget lithography tool.

A 3D nanofabrication of fluidic components by corner lithography particularly to be used in novel tips containing nano-apertures at or near the

apex for AFM-based liquid deposition devices, and a novel particle or cell trapping device using an array of nanowire frames is investigated in Chapter 3.

Next, in Chapter 4, a novel 3D nanowire pyramid as scanning microscopy probe for atomic force microscopy is described using standard micromachining and conventional optical contact lithography.

Finally, Chapter 5 describes the 3D nanofabrication of components by repeated corner lithography to implement self-aligned sub-30 nm nanoapertures and nanowires.

Chapter 2

Wafer-scale Fabrication of Nanoapertures Using Corner Lithography

2.1 Introduction

Micromanipulators with integrated tiny apertures for submicron modification or sensing of surfaces are essential components in the state-of-the-art and emerging nanotechnology. Application fields of apertures include Near-field Scanning Optical Microscopy (NSOM) to study molecules in their native environment (Synge, 1928; Pohl et al., 1984; Heinzelmann and Pohl, 1994; De Serio et al., 2003), fluidic probes e.g. to study the electrophysiology of single cells such as in Scanning Ion-Conductance Microscopy (SICM) (Hansma et al., 1989; Korchev et al., 2000; Miragoli et al., 2011) or to shape surfaces at the nanoscale using electrochemical deposition (Deladi et al., 2005; Staemmler et al., 2002; Kaisei et al., 2011). Apertures are also useful in DNA and single cell devices for screening or sequencing purposes (Dekker, 2007; Branton et al., 2008; Ma and Cockroft, 2010), and Next Generation Lithography equipment to further extend the resolution limit of optical exposure tools (Wegscheider et al., 1995; Tseng, 2007). Furthermore, the use of submicron apertures for fluid delivery can overcome the limitation of the Dip Pen Lithography (DPL) (Piner et al., 1999; Salaita et al., 2007), i.e. the necessity of fluid replenishment and inevitable realignment procedures during a patterning process. Especially, the Fountain Pen Lithography (FPL), which might replace DPL, is of interest here (Lewis et al., 1999; Meister et al., 2003; Deladi et al., 2004, 2005; Kim et al., 2005).

Even though the art of aperture engineering has a long history of developments, it has passed a few turbulent decades of innovation with the introduction of nanofabrication. In the early days, before 1990, the aperture probes were mainly hollow glass pipettes. However, ongoing developments have led to silicon micro- or nanofabricated counterparts that greatly improves its performance: besides ultra-small apertures (Tong et al., 2004a; Sinno et al., 2010; Håkanson et al., 2003; Bruinink et al., 2008; Woldering et al., 2008; Unnikrishnan et al., 2008) nanofabrication allows for device integration, such as combining them with micro-channels and micro-reservoirs to deliver fluids (de Boer et al., 2000; Rusu et al., 2001; Tas et al., 2002; Haneveld et al., 2003; Tong et al., 2003; Haneveld et al., 2008; Unnikrishnan et al., 2009c,a). Furthermore, it enables arrays of probes for parallel operation and batch processing (Tilmans et al., 2001). Moreover, arrays of tiny apertures are useful in supporting extremely thin membranes. This facilitates fast and selective molecular transport via diffusive or free molecular mechanisms (Tong et al., 2004b, 2005a; Hoang et al., 2004; Tong et al., 2005b; Unnikrishnan et al., 2009b).

Nanofabrication rests on the planar photo lithography - which is the main driving force behind the ever decreasing size of the devices - to fulfill automated mass production that achieves astonishing low per-device costs. The construction of wafer-scale full 3 dimensional (3D) nanofeatures, though, is challenging. For instance, the creation of a sub-100 nm aperture at the apex of a tip is not at all straightforward in the planar lithography due to alignment and step coverage issues. Self-aligned schemes have the ability to overcome this problem (Haneveld et al., 2006; Zhao et al., 2008, 2009b,a, 2010). The corner lithography method (Sarajlic et al., 2005; Berenschot et al., 2008; Yagubizade et al., 2010; Burouni et al., 2011, 2012b; Berenschot et al., 2012, 2013), which is applied in this paper, is an example of such a self-aligned technique.

In the established micro system technology, two complementary wafer-scale approaches to create self-aligned sub-micron apertures can be distinguished (Figure 2.1). In the oldest technique, the aperture is formed at the tip-end of a previously fabricated sharp tip (Marcus et al., 1990; Jansen et al., 1995; Sheng et al., 1999; Hübner et al., 2003). The "inverse" technique forms the aperture inside the sharp concave corner of a previously fabricated etch pit, also with a tiny radius (Georgiev et al., 2003; Choi et al., 2003). An example of the "tip-approach" was presented in 1991 by Prater et al. (1991), Figure 2.1A, who used the isotropic undercutting of a micron-sized oxide mask to form a silicon tip and additional boron doping and back-side etch to create a hollow needle. Davis et al. (1995) came with an improved scheme in 1995 by sharpening the tip using wet oxidation (Figure 2.1B). Subsequently,

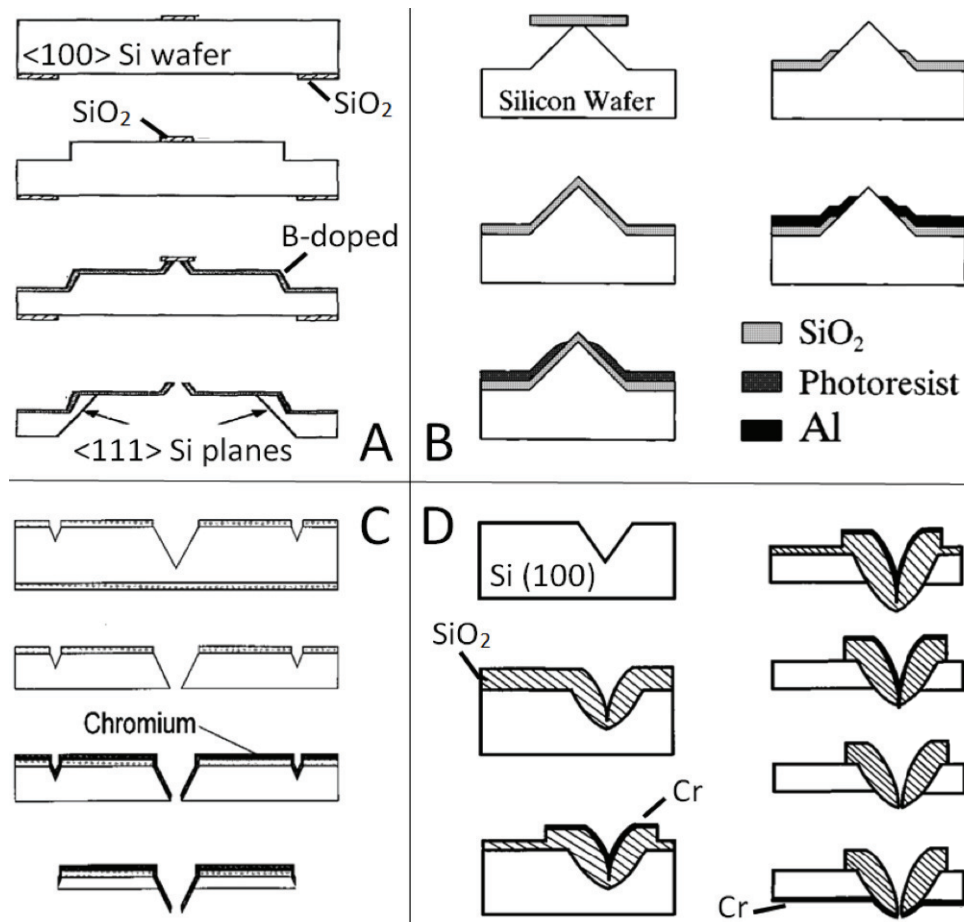


Figure 2.1: Various aperture microfabrication schemes: tip-approach by (A) (Prater et al., 1991) (reprinted with permission, copyright American Institute of Physics 1991) and (B) (Davis et al., 1995) (reprinted with permission, copyright American Institute of Physics 1995), and pit-approach by (C) (Mihalcea et al., 1996) (reprinted with permission, copyright American Institute of Physics 1996) and (D) (Minh et al., 1999) (reprinted with permission, copyright American Institute of Physics 1999).

the tip-end was opened from the front-side using the incomplete coverage of resist due to de-wetting at the sharp tip-end. However, this procedure resulted in a rather unpredictable aperture size.

This issue improved after the introduction of the pit approach in 1996 by Mihalcea et al. (1996), Figure 2.1C, in which a sharp etch pit was used as a template to construct the aperture. The pit typically forms following the anisotropic etch characteristics of crystalline silicon in hydroxide-based solutions (Oosterbroek et al., 2000; Berenschot et al., 2009). Even though

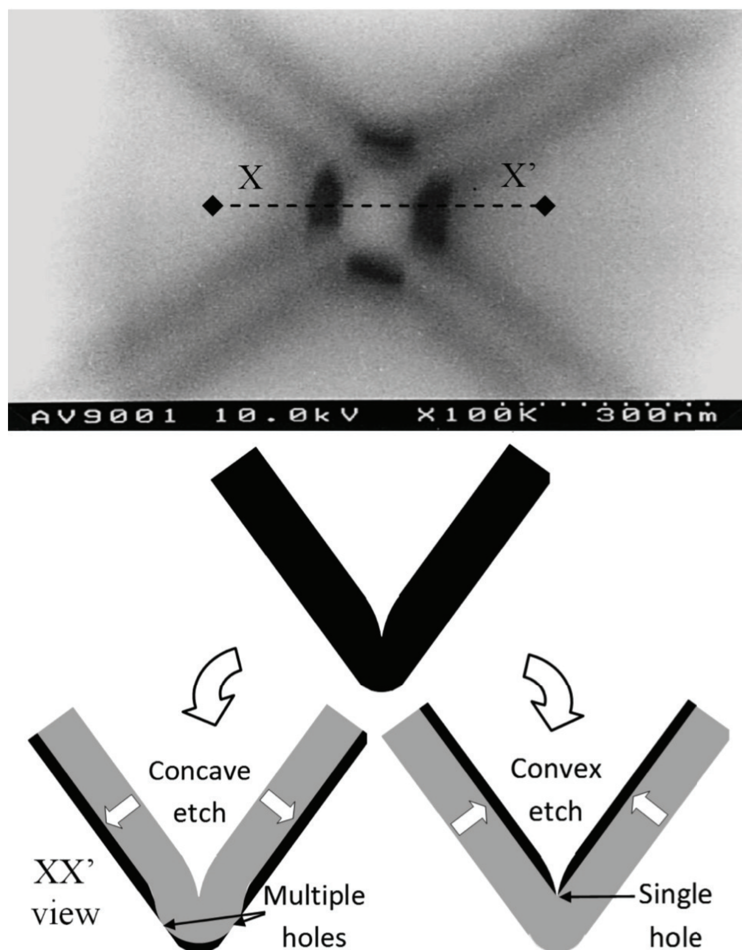


Figure 2.2: Isotropic etch-back of oxide in etch pits. Top: Mihalcea et al. (2000) (reprinted with permission, copyright The Electrochemical Society 2000) showing a four-fold aperture. Left: concave side etch resulting in tip broadening (Mihalcea et al., 2000) (reprinted with permission, copyright The Electrochemical Society 2000). Right: convex side etch forming a sharp single aperture (Minh et al., 1999) (reprinted with permission, copyright American Institute of Physics 1999).

submicron apertures were achieved, they improved the technique in 2000 to sub-200 nm resolution by the effect of oxidation retardation at the concave corner of the etch pit (Mihalcea et al., 2000). The effect is essentially identical to the previously mentioned oxidation-based sharpening technique. A disadvantage, though, of this concave etch technique is that resolution is limited due to oxide thinning near, but not at, the tip-end (Figure 2.2.top and bottom-left). It results in apertures having difficulties to achieve sub-100 nm resolution. However, meanwhile a further improvement of the aperture size

was presented in 1999 by Minh (Minh et al., 1999) who thinned down the oxide using an isotropic etch from the convex side (Figure 2.1D and Figure 2.2.bottom-right). In this way sub-25 nm apertures were created successfully.

In this chapter, an alternative technique to create 3D nanostructures and apertures (and tips) at sharp corners (in fact the apexes of micromachined pyramidal shapes) is presented with the general aim to achieve high resolution throughout the wafer, while allowing freedom to create apertures with characteristic dimensions up to a few hundreds of nanometer. It has the advantage, with respect to the established techniques shown in Figure 2.1, that the apertures are formed prior to the aperture release (like the tip-approach), but still has the ability to reach sub-50 nm apertures (like the pit approach). Furthermore, in the current approach additional freedom in aperture size is achieved, as compared with Minh's approach, mainly because the latter has to rely on the effect of oxidation retardation caused by the angle of the concave corner and the surface orientation. The advantage of the presented technique with respect to Milhalcea's approach (of using the deposition of nitride instead of the growth of oxide) is that multiple aperture "ghost" holes are prevented and, therefore, an increased resolution is possible. As the others, the technique is fully compatible with standard micromachining methods and, as such, it does not rely on mainstream sub-100 nm nanolithography tools. It is based on the so-called corner lithography technique, as will be explained in detail in section 2.2.

Corner lithography was introduced by Sarajlic et al. (2005) and was used to create a nanowire frame (Figure 2.3) and a brief theoretical foundation for a simplistic 2 dimensional shape (V-groove) was formulated. In 2008, Berenschot et al. (2008) extended this work with a few other 3D structures, such as a pyramid with a metal nanotip. In 2010, Yagubizade et al. (2010) presented corner lithography as a tool to construct silicon nanowires and in 2012 Berenschot et al. (2012) used corner lithography to construct wireframes able to catch living cells. Most recently, Berenschot presented a new class of structures - octahedral fractals - having the potential to fabricated extreme porous or large area membrane devices (Berenschot et al., 2013). The fractals were fabricated with the aid of anisotropic etching of silicon in combination with the self-aligned 3 dimensional corner lithographic technique. The fractals demonstrated were dense, porous, as well as a wireframe. However, in neither case details on the 3D size of these nanostructures were given. To summarize, the objective of this chapter is to demonstrate the main concept of corner lithography and to present some fundamental issues controlling the aperture shape and size. Results from statistical data on the wafer-scale uniformity supports this study.

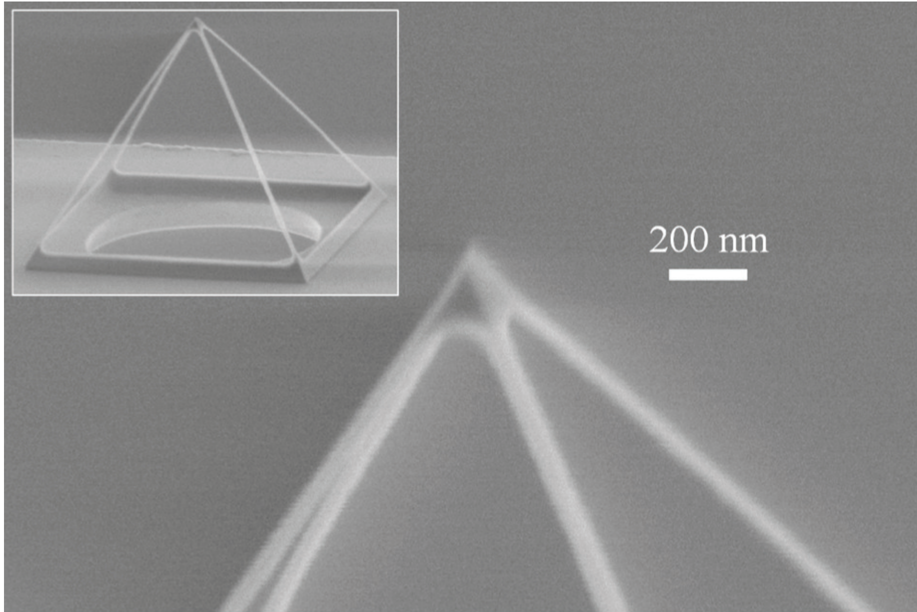


Figure 2.3: Pyramidal wire frame (Sarajlic et al., 2005). The wires are roughly 100 nm in width.

2.2 Corner Lithography Concept and Theory

Figure 2.4 illustrates the basic corner lithography scheme, which is compatible with conventional micromachining techniques. I) It starts with the definition of micron-sized patterns using print lithography. For example, a $< 100 >$ silicon wafer is oxidized and patterned with a resist mask having a micron-sized grating pattern. After pattern transfer using BHF and resist stripping, the oxide is used as a mask to etch the silicon anisotropically using a hydroxide-solution and forming V-grooves bounded by slowly etching $< 111 >$ planes (Oosterbroek et al., 2000; Berenschot et al., 2009). For silicon, the concave angle α between these planes will be ca. 70.53°. II) Next, a thin conformal layer of silicon nitride is deposited in this silicon template by Low-Pressure Chemical Vapor Deposition (LPCVD). III) Subsequently, the nitride is partly removed (time-stop), leaving a nitride residue in the concave corners. The process results in well-defined nanometer-scale structures controlled by the template. The remaining material in the corners directly forms the structural material of tips and wire structures or is used as an inversion mask in subsequent fabrication steps to form apertures or slits.

The theoretical analysis of the final width a after etch-back of a filled V-groove is straightforward by solving for the intersection of a circle ($x^2 + y^2 = r^2$) with a triangle ($y = c_1 + c_2 \mid x \mid$) and with the centre of the circle as

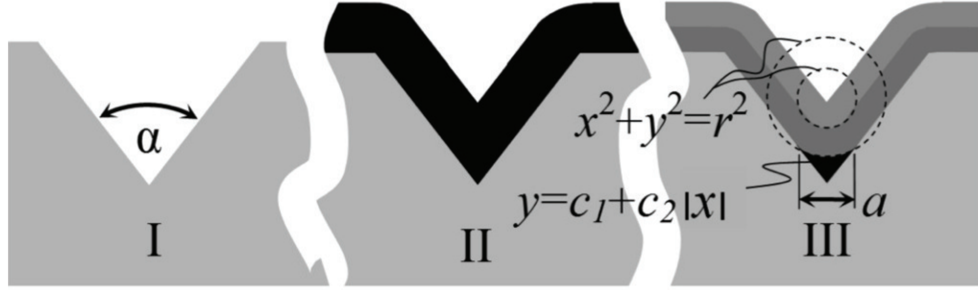


Figure 2.4: Corner lithography concept (cross-sectional view): (I) V-groove template preparation, (II) deposition of conformal material, and (III) time controlled selective isotropic thinning leaving a nano feature of size a. The concave corner angle is defined as α, which is between 0 and π. A different concave angle, layer thickness or etch-back will result in a different feature size and shape.

indicated in Figure 2.4III:

$$\frac{a}{t} = 2\cos(\frac{\alpha}{2}) - 2\sin(\frac{\alpha}{2}).\sqrt{(\frac{r}{t})^2 - 1}. \tag{2.1}$$

The analysis for the 3D case is identical except that we have to equate a sphere with a pyramid, which results in a hyperbolic square. Figure 2.5 and Table 2.1 show how the aperture changes size and shape with the relative amount of material removed.

Table 2.1: Feature size for different corner angles

Angle of corner	Relative feature size
$\alpha = 70.53°$	$\frac{a}{t} = \frac{2}{3}\sqrt{6} - \frac{2}{3}\sqrt{3}\sqrt{\left(\frac{r}{t}\right)^2 - 1}$
$\alpha = 90.00°$	$\frac{a}{t} = \sqrt{2} - \sqrt{2}\sqrt{\left(\frac{r}{t}\right)^2 - 1}$
$\alpha = 109.47°$	$\frac{a}{t} = \frac{2}{3}\sqrt{3} - \frac{2}{3}\sqrt{6}\sqrt{\left(\frac{r}{t}\right)^2 - 1}$

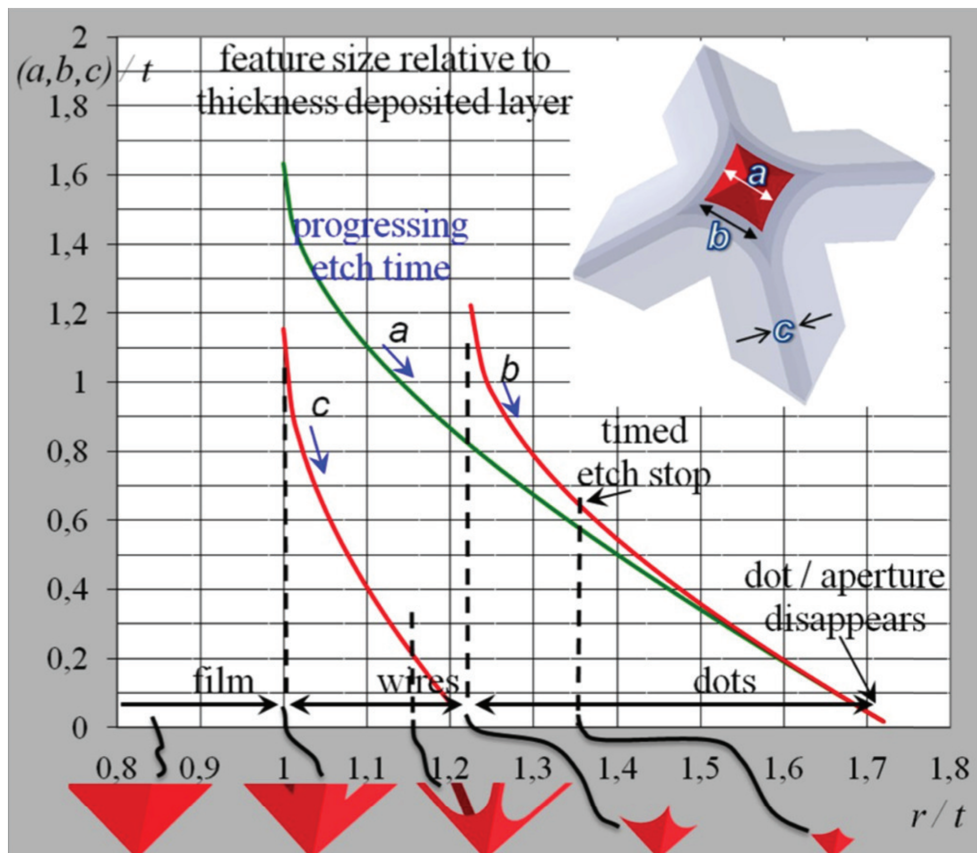


Figure 2.5: Feature size relative to the deposited layer with thickness t, as a function of the relative isotropic etch distance. a is the minimum size of the dot in the apex, b is the maximum size of the dot in the apex, and c is the minimum width of the wires remaining in the ribs of the pyramid.

2.3 Aperture Fabrication

The nanoaperture fabrication (Figure 2.6) starts with a $< 100 >$ silicon wafer coated with 76 nm thermal oxide, which is patterned by conventional resist lithography using a periodic hole pattern (circles of 5 μm). The mask is fabricated with the Heidelberg DWL 2000 laser-beam pattern generator (minimum structure size of 0.8 μm, 25 nm address grid, edge roughness 3σ=80 nm, CD uniformity 3σ=90 nm, and alignment accuracy 3σ=100 nm). The oxide is etched in BHF and subsequently the silicon is anisotropically etched for 6 min in 25% w/w KOH/H_2O at 75°C. RCA cleaning is performed to remove residual potassium ions and the remaining oxide is stripped for 1 min in 50% HF. This forms a silicon template with many inverted pyramids

- the etch pits - having sharp concave corners (Figure 2.6A). The silicon template receives a conformal layer of t=61 nm LPCVD silicon-rich nitride (SiN_x) (Figure 2.6B). Based on the angle of the corners, this will result in a thickness of $t\sqrt{3} \approx 1.73t$ in the apex (α=70.5°) of the pyramid and $\frac{1}{2}t\sqrt{6} \approx 1.22t$ in the ribs (α=109.5°). An etch in 85% phosphoric acid heated up to 160°C (hot H_3PO_4) between 1.00t and 1.22t results in a nanowire pyramid (Sarajlic et al., 2005) (Figure 2.6C, 1.15t) and for the fabrication of a nanodot this is between 1.22t and 1.73t (Figure 2.6D, 1.35t).

To have a safe margin with respect to possible non-uniformity, a relative layer of around 1.35t is removed and a residual nitride dot of around 40 nm is left (Figure 2.5: b-side $\approx 0.65t$). The wafers are HNO_3 cleaned and 54 nm oxide (< 111 > surface) is grown by dry oxidation for 20 min at 1050°C in which the nitride dot serves as an inversion mask; i.e. the local oxidation of silicon (LOCOS, Figure 2.6E). After removing the oxidized nitride for 30 sec in 1% HF, the nitride is stripped in hot H_3PO_4 with 35% extra time (Figure 2.6F). A thin oxy-nitride transition layer of ca. 3 nm, grown during loading the wafers in the LPCVD furnace, (Tanaka et al., 1999) is stripped for 45 sec in 1% HF. Finally, the wafer is bonded to a second patterned wafer and stripped from the silicon to reveal apertures with fluid access holes through the second wafer or it is bonded to a glass tube and then the silicon is stripped (Figure 2.6G) (Unnikrishnan et al., 2009c,a). The aperture is drawn not to scale with respect to the glass tube.

2.4 Results and Discussion

The fundamental assumption of corner lithography is that the isotropic etch rate is the same for a flat surface and a concave corner, whether it is a V-groove (Figure 2.4) or an inverted pyramid (Figure 2.6). More important, in order to predict the aperture size at the apex of the pyramid (Figure 2.6F), the isotropic etch of the nitride inversion mask has to be controlled. Two etchants have been studied; hot phosphoric acid (H_3PO_4) and 50% hydrofluoric acid (HF) at room temperature. In silicon micro-machining, typically a hot H_3PO_4 solution is used as it has a reasonable selectivity with respect to silicon and silicon dioxide, which are common materials present during silicon-based etching. However, when the presence of oxide is not important, 50% HF is favored because silicon is virtually undisturbed in pure HF solutions (Haneveld et al., 2008). An important issue addressed in this paper is to find the characteristics for both etchants. For this, the wafer-scale thickness uniformity (mean value and standard deviation) of the initial nitride layer, the remaining layer after the isotropic etch, and the final aperture size is

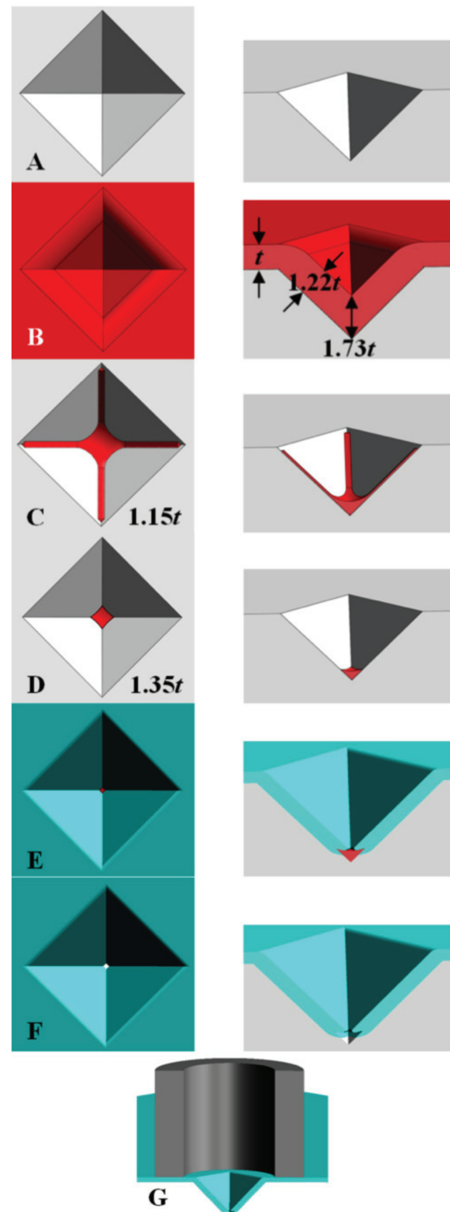


Figure 2.6: Fabrication process of a 3D aperture. Left panel top view and right panel bird view: A) pit formation using a patterned SiO_2 mask and KOH, B) conformal deposition of SiN_x of thickness t, C) etch-back of 1.15t with HF or H_3PO_4, D) etch-back of 1.35t, E) LOCOS using nitride dot, F) nitride strip, G) bonding with a second wafer patterned with access holes and aperture release (not to scale).

estimated in the coming sections. Non-patterned (dummy) wafers and ellip-

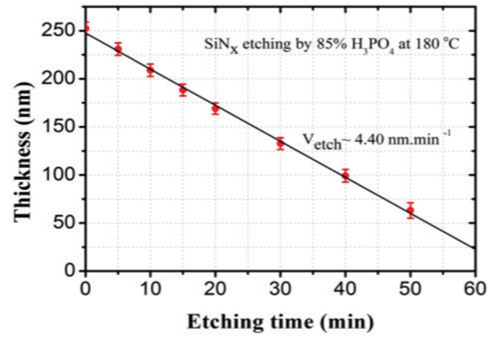
sometry are employed to subtract the global etch rate and wafer uniformity. Processed wafers with V-grooves, which received an identical treatment, are used to check these values. Finally, the shape and size of the apex aperture is examined with high resolution scanning electron microscopy HRSEM.

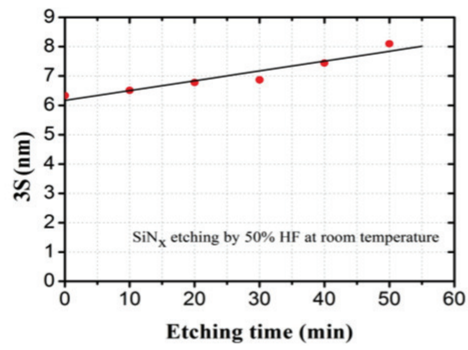
2.4.1 Uniformity of Non-patterned Wafers

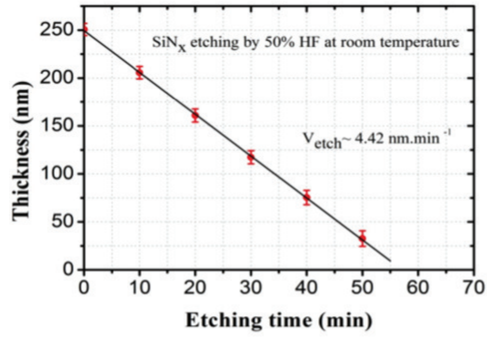
Native oxide was stripped from < 100 > silicon wafers in 50% HF. Subsequently, the wafers were coated with 250 nm nitride. The nitride was isotropically etched by hot H_3PO_4 and the remaining thickness was measured every 10 min using ellipsometry at 25 uniformly distributed spots across the wafer. The experiment was repeated with 50% HF. Figure 2.7 shows for both etchants the thickness t of the remaining nitride layer and estimated standard deviation S_t as derived from the measured n = 25 spots against time and defined as:

$$S_t = \sqrt{\frac{\sum_{i=1}^{n}(t-\bar{t})^2}{n-1}}, \tag{2.2}$$

in which t is the value of every individual measured spot and $\bar{t}$ is the average of these values. Before etching, the deposited nitride is quite uniform ($3S_t \approx 6$ nm out of 250 nm, i.e. better than 3%), but during etching the estimated standard deviation in the thickness of the remaining layer increases due to local variations in the etch rate. This local variation can be due to differences in the nitride film density or another property or can come from fluctuations of etch species concentration and temperature of the wet etchant. Furthermore, the etch rate for 50% HF is around 4.4 nm/min and that of hot H_3PO_4 is roughly 3.8 nm/min. The observed variation in the local etch rate causes a $3S_t$ error in the remaining layer of $0.04t$ after etching a layer of $1.35t$ (in order to create a nanoaperture), so it is possible to etch accurately enough to be well within the required range of $1.22 \leq 1.35 \pm 0.04 \leq 1.73$ for the nanodots to exist. Furthermore, the control of the size of the final aperture becomes better, the closer the required aperture size is to the nitride thickness deposited initially. Creating a small aperture by starting with a relative thick layer and etching a bit longer in the corner lithography (e.g. for $1.60t$) will result in larger spread of the aperture size due to the increase of the relative non-uniformity with etching time. However, it is recommended not to restrict the over etch time too much below 35%. The reason is that inaccuracy of the etch rate (the slopes of the curves found in Figure 2.5 get steeper at less relative etch-back time) and depletion in small confined structures may even cause that the wires do not disappear, which excludes







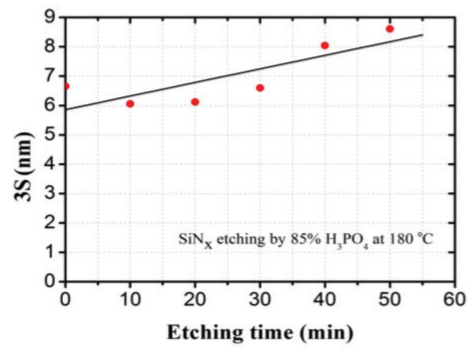


Figure 2.7: Global SiN_x etching in 50% HF and hot H_3PO_4.

apertures to form correctly.

2.4.2 V-grooves

Wafers with V-grooves (like Figure 2.4) and flat dummy wafers were coated with 250 nm SiN_x and etched in the same bath to remove 0, 100, 150, 250, 308, 338 and 375 nm ($0.0, 0.4, 0.6, 1.0, 1.23, 1.35$ and $1.50t$ respectively). Subsequently, the remaining nitride shape and etch uniformity at the apex was observed by HRSEM (Figure 2.8). The same etch rate was found at the inclined wall of the V-groove, compared with that of the flat surface of the dummies. This indicates that the size of the remaining nitride in the concave corners can be predicted accurately. Also, the shape of the material left is as expected for etching in hot H_3PO_4, but it shows a deviation for etching in 50% HF. As indicated in Figure 2.8 with the arrows, the etch-front follows a kind of cosine shape. A possible explanation is that a thin oxide is grown unintentionally during loading the wafers in the hot LPCVD tube (Tanaka et al., 1999). Delayed deposition (causing oxide to grow) as well as flushing with ammonia gas (causing oxide to convert into nitride) both influence the final native oxide thickness. This oxide or oxy-nitride transition layer is eroded faster in 50% HF than the intended nitride layer.

In Figure 2.9, a nitride nanowire situated in the corner of the V-groove is shown. The silicon surrounding the wire is partly etched anisotropically to have a better view with respect to the shape of the wire. It is good to mention that this extra silicon retraction etch causes two nanometer-sized V-grooves to appear adjacent to the original V-groove. Oxidizing this structure or doing once again nitride deposition and partly etch-back might show even more exciting nanostructures with sub-100 nm resolution. The reader is encouraged to explore this possibility further, but in this work we go back to the basic aperture process flow.

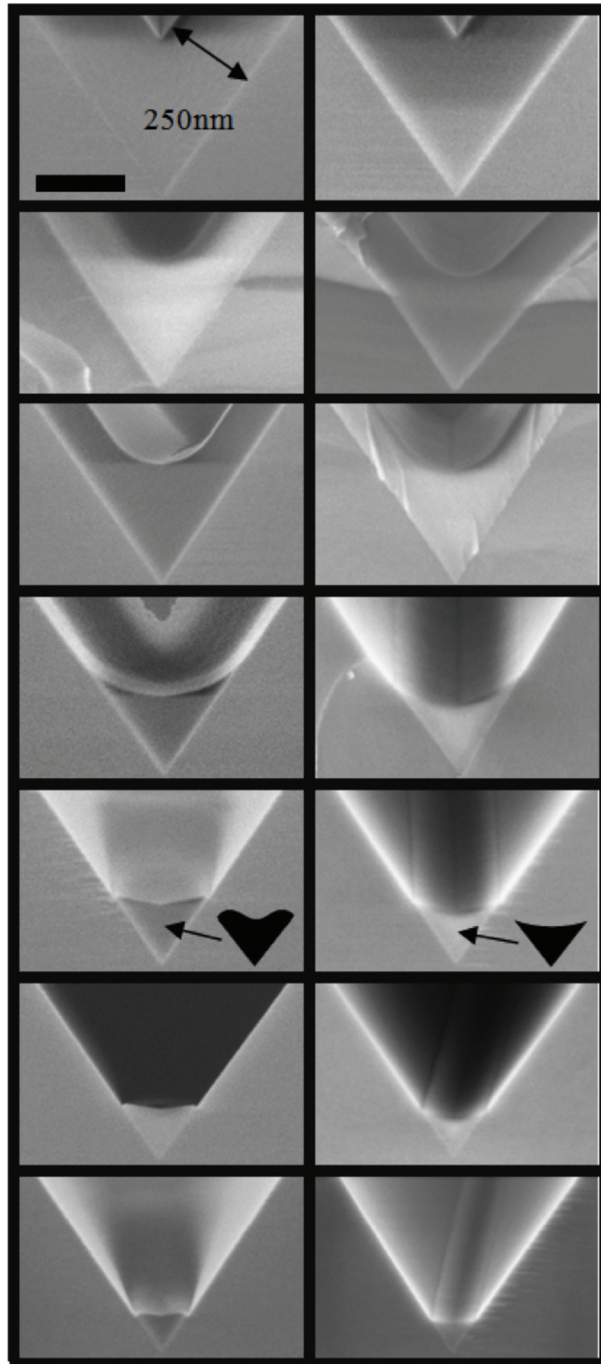


Figure 2.8: Nanofeatures in a corner ($\alpha = 70.5°$) after time-stopped etching ($0.00t, 0.40t, 0.60t, 1.00t, 1.23t, 1.35t$ and $1.50t$) with 50% HF (left) and hot H_3PO_4 (right). The bar in the picture represents 250 nm.

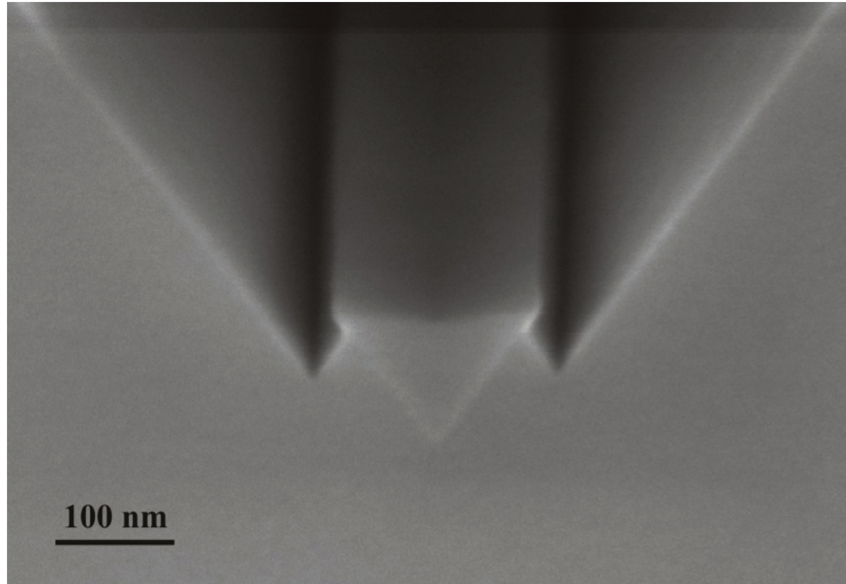


Figure 2.9: Nitride nanowire after hot H_3PO_4 etch ($1.23t$) in a V-groove prior to LOCOS inversion. The silicon is partly etched anisotropically to observe the shape better.

2.4.3 Apertures

Series of inverted pyramids are defined as discussed in section 2.3. The nitride layer is etched with a 135% etch time in hot H_3PO_4, leaving nitride dots in the apexes. The over etch was controlled by separate dummies. Figure 2.10 shows a dot after an additional anisotropic silicon etch but, like the V-grooves, starting with a rather thick 250 nm nitride. The hyperbolically sharpened 200 nm features are as expected for corner lithography. For the sub-50 nm apertures, a thinner layer of 61 nm nitride has been selected. After LOCOS and nitride strip, including the 3 nm oxy-nitride transition layer, the silicon is etched in TMAH solution. This leaves an aperture at the apex of the pyramid as can be seen in Figure 2.11. The opening measures 44 nm by 55 nm and it is not truly a (hyperbolic) square as one might expect. This issue is addressed by Moldovan et al. (2012) *"Optical lithography can control the equality of adjacent sides of squares or circle eccentricities only down to 20-50 nm, due to factors such as illumination non-uniformities, mask imperfection, proximity effects in the aerial image, and concentration gradients in the developer...Thus, the wedge size on four-faceted pyramidal molds can be controlled only to the limit of tens of nanometers"*. Figure 2.12 shows a top view of the inverted pyramid just before removing the 76 nm thermal oxide mask. It can be seen that the circular distortion matches the

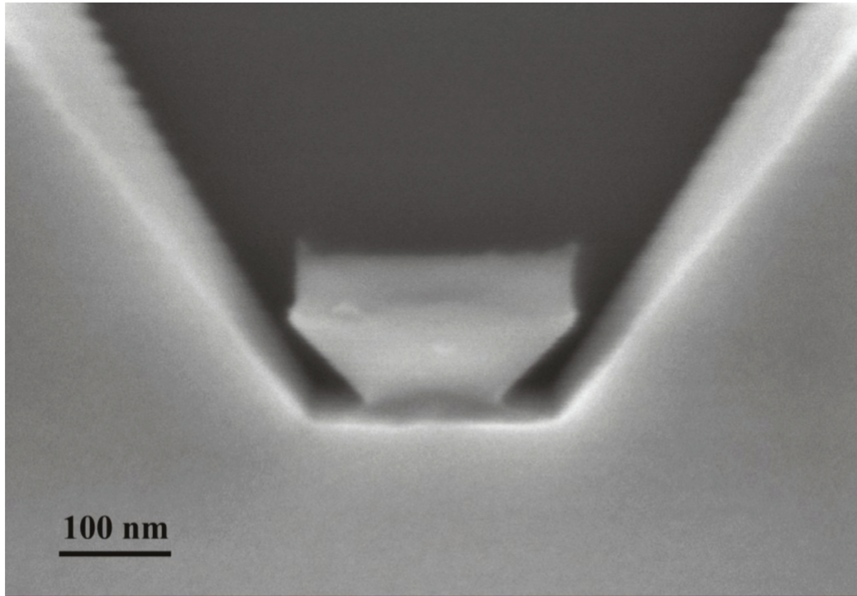


Figure 2.10: Nitride nanodot at the apex of an inverted pyramid prior to LOCOS inversion. The silicon is partly etched anisotropically to observe the shape.

wedge length.

To proof the wafer-scale ability of corner lithography, a detailed statistical analysis has been done for a total population of 50 million apertures. For this, five spots were quasi-randomly selected to investigate the 100 mm wafer uniformity. One in the centre of the wafer, one north and 1 cm away from the periphery. The other three east, south and west, also 1 cm from the wafer edge. HRSEM pictures were taken at a fixed magnification of 5000 times, which resembles an area of $60\mu m \times 40\mu m$ and containing 20 oxide pyramids with apertures. From every spot, six apertures were randomly selected for a high resolution picture at a fixed magnification of 200.000 times and the aperture size was measured within seconds to minimise carbon deposition while scanning. Figure 2.13 shows the size variation of some apertures situated close together on the wafer. Table 2.2 presents the data on wafer-scale. Taking only the centre spot, the size of the smallest b-side is found to be 43.8 nm with an estimated standard deviation (s_{N-1}) of 1.2 nm. The longest b-side is 71.5 ± 66.7 nm. The latter means that pattern imperfections have created knifes (or wedges) of 27.7 ± 67.1 nm. This number corresponds well with the given CD uniformity of the pattern generator to create the mask: σ=30 nm. Taking the average size of all the $N = 30$ samples across the wafer, the smallest side is calculated to be 44.5 ± 2.3 nm and the longest side: 71.4 ± 91.3 nm. The precision uncertainty of the smallest b-

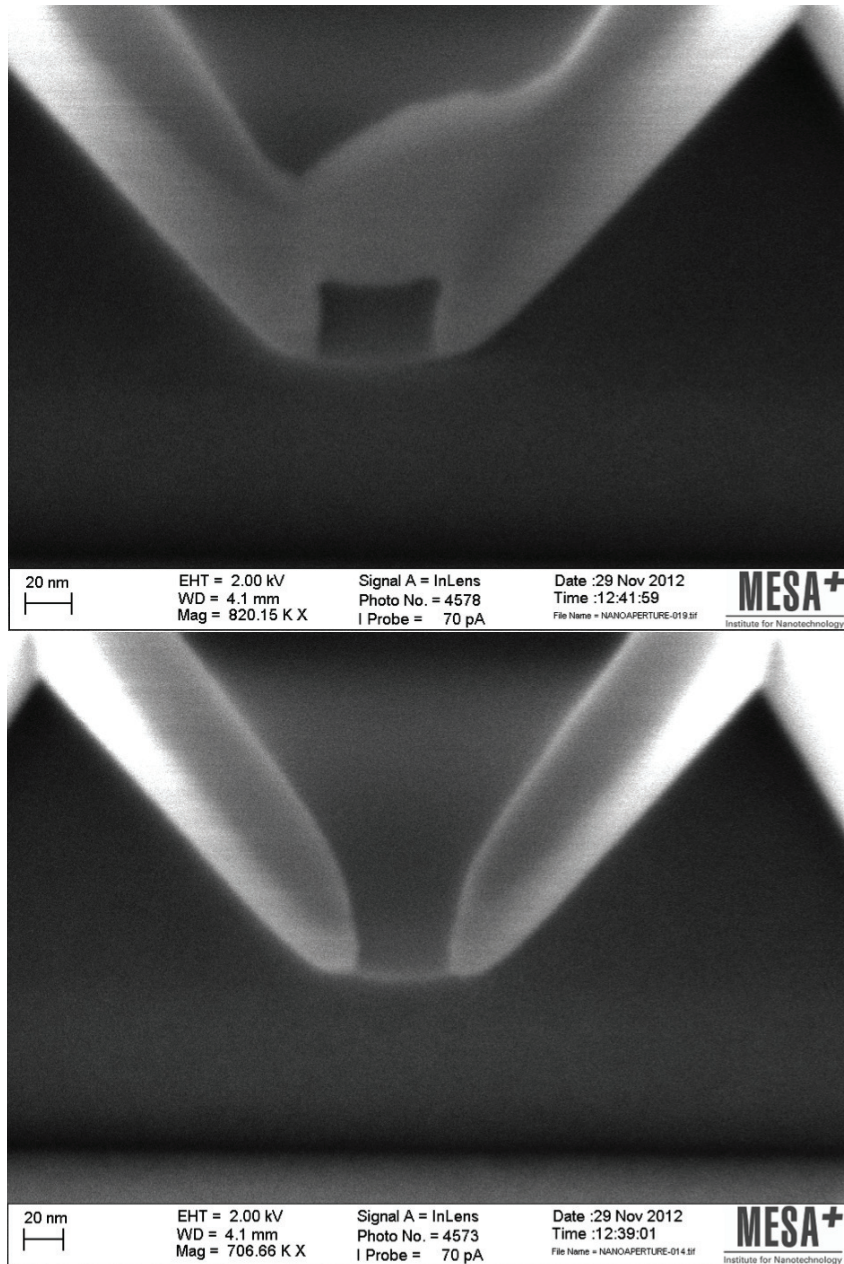


Figure 2.11: Aperture of $44nm \times 55nm$ inside an oxide frame (bird's eye and side views) after corner lithography in a pyramidal etch pit. The aperture is not a perfect square but has a hyperbolic rectangular shape (Hübner et al., 2003). The lips along the sides are a consequence of the corner lithography as found in Figure 2.5.

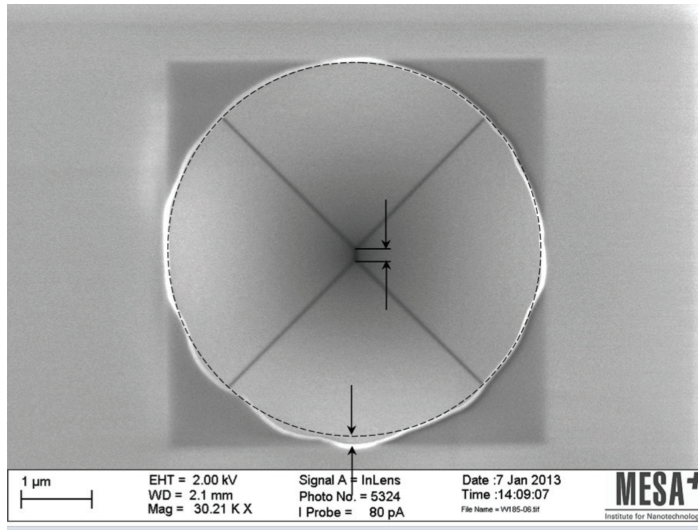


Figure 2.12: Imperfection of the mask shape causing a wedge to develop. The dashed line is a perfect circle.

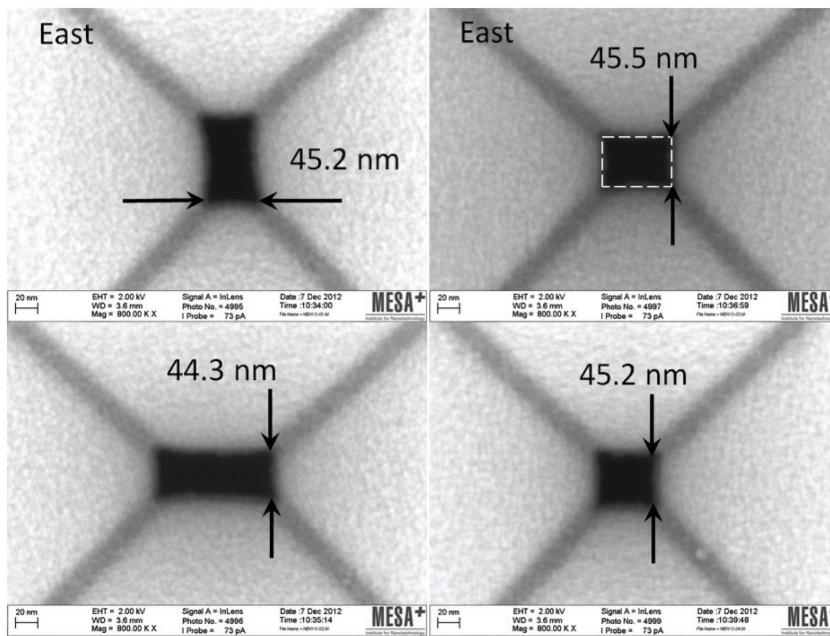


Figure 2.13: Variation of the size of four apertures (exact top view) taken at the east position of the wafer. The apertures are situated close together in an area of 40 by 60 microns. The white dashed rectangular shape is enclosing exactly the limits of the aperture; i.e. the b-sides. The smallest side is always around 44 nm whereas the longest side has a large variation.

side is therefore (in Excel) $P_b = TINV(0,05;29) \times s_{N-1} = 2.045 \times 2.3 = 4.6$ nm, where TINV is the Student t-distribution variable at the 95% confidence level with $N-1$=29 degrees of freedom (Alder and Roessler, 1962; Fisher, 1926; Gosset, 1942). Indeed, taking a closer look at values for the smallest b-sides in table 2, only 1 value does not fit within the range between 39.9 (44.5-4.6) and 49.1 (44.5+4.6) nm. So, it can be concluded that the smallest side is highly reproducible on the wafer-scale and that corner lithography is sufficient accurate. This is a direct result of the ability of anisotropic etching to create very sharp edges where $< 111 >$-planes meet. However, the longer side of the apertures is very inaccurate (large standard deviation). The reason is most probably the lack of sufficient symmetry control of the original mask (the pretended circles are always distorted as previously shown in Figure 2.12). Finally, having a closer look at Table 2.2, the mean value of smallest b-sides of the North position (41.7 nm) is less than that of the South position (47.3 nm). We believe that this is caused by a temperature gradient in the H_3PO_4 bath. Furthermore, the "predicted" minimum size of 40 nm is approximately 4 nm less than observed. We believe that the 6 nm oxy-nitride layer has caused this offset.

Table 2.2: Aperture size (length l and width w in nm) at different wafer positions (North, West, Centre, East, and South). The value of the longest b-side is taken negative in the statistical analysis when the ridge is 90 degrees rotated with respect to the most frequently found direction.

N	l	42.9	41.4	43.6	40.0	-119.3	40.0
	w	66.2	102.4	85.5	221.0	42.1	140.2
W	l	44.3	-79.0	42.9	-85.2	45.7	-100.0
	w	159.3	46.0	107.6	44.8	143.3	46.2
C	l	41.9	45.5	43.8	43.3	43.8	-58.6
	w	97.9	64.3	106.7	94.3	124.5	44.3
E	l	-79.0	44.3	45.5	45.2	43.1	45.7
	w	45.2	104.8	64.0	53.3	238.6	138.6
S	l	49.0	47.9	49.3	47.9	45.0	44.5
	w	66.9	115.0	100.7	138.3	66.2	63.6

2.5 Conclusions

We have investigated a wafer-scale method to obtain three dimensional nanostructures, called corner lithography. The technique explores the conformal deposition and subsequent timed isotropic etching of a thin nitride film into a very sharp etch pit; the latter serving as a template. This leaves a small nitride residue in the pit's corner, which is used as a self-aligned mask with high resolution ability to oxidize the free-accessible silicon. This residual nitride dot is selectively removed to create the nanoaperture at the tip apex. A size of below 50 nm is demonstrated, but potentially it allows even smaller openings. The advantage of this method in aperture fabrication over existing wafer-scale methods is the large possible range of sizes of the aperture while the structure is still in the mould. This gives flexibility in further machining steps.

Chapter 3

3D Nanofabrication of Fluidic Components by Corner Lithography

3.1 Introduction

The advent of microelectronics in the 1960's has resulted in a multitude of electronic but also mechanical and fluidic micro-components. The functionality of micro and nanostructures can be greatly enhanced if nano-patterning techniques can be applied to non-planar objects and at surfaces that are arbitrarily oriented in space. An example of such a technique is focused ion beam (FIB) milling (Reyntjens and Puers, 2001) in which the focused ion beam can be applied to any spot on a 3D micro-object. However, when large numbers of objects have to be machined, the disadvantage of this technique is the intrinsic serial nature. Corner lithography (Sarajlic et al., 2005; Berenschot et al., 2008; Yu et al., 2009) is a wafer scale nano-patterning technique that has the interesting property that it forms nanostructures in sharp concave corners, independent of their orientation in space. This is a consequence of the isotropic nature of the two basic steps involved: conformal deposition followed by isotropic etching. Figure 3.1 illustrates the principle of corner lithography at the intersection of two planes. After conformal deposition of a layer of thickness t the effective thickness in the corner is $a = t/sin(\alpha/2)$, where α is the angle of the concave corner. After isotropic thinning by an amount of r the remaining material in the corner will have a thickness $b = a - r$ (Sarajlic et al., 2005). If the corner is formed by the intersection of two planes the resulting material will constitute a nanowire, if the corner is formed by the intersection of three or more planes a nano-dot will be formed, possibly connected to a frame of nanowires formed in the corners between intersecting pairs of planes. Corner lithography was initially developed in our

lab by Sarajlic et al. (2005) who created a silicon nitride nanowire pyramid. Berenschot et al. (2008) investigated the use of structures formed by corner lithography as a mask material in subsequent steps. Yu et al. (2009) independently developed corner lithography and applied it for the fabrication of nano-ring particles and photonic crystals.

Figure 3.1: Corner Lithography concept (cross-sectional view): (I) V-groove template preparation, angle α, (II) deposition of conformal material, layer thickness t and thickness a in the corner, and (III) time controlled selective isotropic thinning by distance r leaving a nano feature of height b.

In the current work, we introduce the fabrication of nano-apertures by corner lithography, and show the integration of corner lithography based structures in microfluidic devices. The basic functionality of these devices is demonstrated. In the most advanced application, we show the feasibility of using these structures to separate individual primary chondrocytes in 2D while maintaining their 3D spherical morphology. Corner lithography can be used as a wafer scale method for obtaining apertures at the apex of micro-pyramids, or near the apex of these pyramids ("side-apertures"). These modified pyramids can be applied as functional tips in Atomic Force Microscopy (AFM) based liquid deposition techniques, such as dip-pen nanolithography (DPN) (Piner et al., 1999), Nano-Scale Dispensing (NADIS) (Meister et al., 2004, 2003; Fang et al., 2006), and fountain pen based lithography (Deladi et al., 2004; Kim et al., 2005). An emerging application of fluidic AFM is in single cell biological or biophysical experiments (Dörig et al., 2010). Pyramids containing nano-apertures could find application as advanced electrospray emitters for the generation of nano-scale droplets (Arscott and Troadec, 2005). In a wider perspective, well-defined nano-apertures can be applied in DNA translocation experiments (Dekker, 2007; Branton et al., 2008; Ma and Cockroft, 2010; Schneider et al., 2010), and in nano-filter devices (Kuiper et al., 1998; Tong et al., 2004a; Holt et al., 2006).

In addition, we used the parallel nature of corner lithography to create arrays of silicon nitride nanowire pyramids in a perforated membrane to form

a single cell trapping device. By using these flat arrays of pyramids, cells can be distributed in a predefined pattern while preserving their natural 3D morphology. An ultimate cell culture device is created by melting a glass tube on top of these arrays (Moğulkoç et al., 2009; Unnikrishnan et al., 2009a). These pyramid arrays where then used for capturing single chondrocytes, capturing each individual cell in one single pyramid. We observed that trapped cells maintained their initial rounded morphology and an increasing amount of filopodia-like structures were protruding from these entrapped cells during the first days after cell seeding. This proofs that these cells were metabolically active. Based on the aforementioned results we show that by corner lithography one can not only batch-wise produce functional AFM tips, but also a platform to study single cells in vitro in a 2D array of nanowire pyramids, in which they maintain their three dimensional phenotype.

3.1.1 Control of Meniscus Size in AFM-based Deposition

A crucial issue in all AFM based deposition processes is control over and reduction of the lines or dots written. This is closely related to the size of the meniscus formed at the tip-substrate contact spot (Piner et al., 1999). However, this is not the only factor. Also the dependence of the surface diffusion on relative humidity (RH) plays an important role (Schwartz, 2002). In fountain pen lithography (Deladi et al., 2004; Kim et al., 2005) and NADIS (Meister et al., 2004, 2003; Fang et al., 2006), a local environment with a high vapor pressure is formed by the supply of ink, or a bulk liquid flow is supplied all the way to the apex. In both processes, limiting the size of the meniscus formed by guiding the ink through a nano-structured tip can be beneficial for the control of the resolution. This is the rationale behind creating side-apertures near the apex of the pyramidal tip (section 3.2.1). In the NADIS process, a droplet of ink is deposited in the back of the hollow pyramidal tip. Liquid is transferred to the substrate through a hole at the apex of the pyramid, which is commonly machined by FIB. Machining the aperture in a wafer-scale process would be desirable because it provides many more probes at much lower cost. Potentially it also increases the reproducibility of the aperture size. The aperture size plays a crucial role in the deposited feature size (Fang et al., 2006). In section 3.2.1 we introduce a wafer-scale procedure to fabricate a nano-aperture at the tip apex.

3.1.2 Cell Trapping Devices

Cell trapping is a crucial step in many innovative biological experiments like electroporation, patch clamping, and drug injection (Andersson and Van den Berg, 2003). The main trapping mechanisms reported are mechanical and di-electrophoretic (DEP) trapping (Andersson and Van den Berg, 2003). Mechanical traps include weir-type filters (Wilding et al., 1998; Yang et al., 2002), pillar based filters (Andersson et al., 2000), and perforated membrane based filters (Huang and Rubinsky, 2001). A common feature of these traps is that the cells are captured in a relative closed environment, which may influence their properties. An indication of this is given by Randall et al. (2011), who created 3D microwell arrays for cell culture. They showed that perforating the walls of the 3D wells increases cell viability as well as insulin secretion of β-cells in response to a glucose stimulus. While Randall et al. (2011) created 3D wells for clusters of cells, in the current work we focus on 3D open traps for single cells based on nanowire pyramidal structures (section 3.2.2).

3.2 Results and Discussion

3.2.1 Nano-apertures Near or at the Apex of a Micro-pyramid

In this section we present two nano-fabrication procedures: one to form an aperture at the apex of a micro pyramid, and one to form side-apertures near the apex of the pyramid. The first procedure focuses on the fabrication of the nano-aperture only, and is illustrative for the formation of a nano-structure in the intersection of more than two planes. The second procedure combines this basic scheme with a second important technique: retraction etching to form a nano-structure at an edge or contour (Gates et al., 2005; Zhao et al., 2009b). The pyramids fabricated following this second procedure were integrated with cantilever beams, which made it possible to handle them and place them in contact with a substrate. The contact point was studied in detail in an environmental scanning electron microscope (ESEM) to follow the formation of the water meniscus for different tip geometries.

Nano-aperture at the Apex of a Pyramid

In brief, to form an aperture the material that is created in the apex of a pyramidal mold by corner lithography is first used as a mask in an inversion step, and subsequently removed. Finally, the silicon mold is removed to

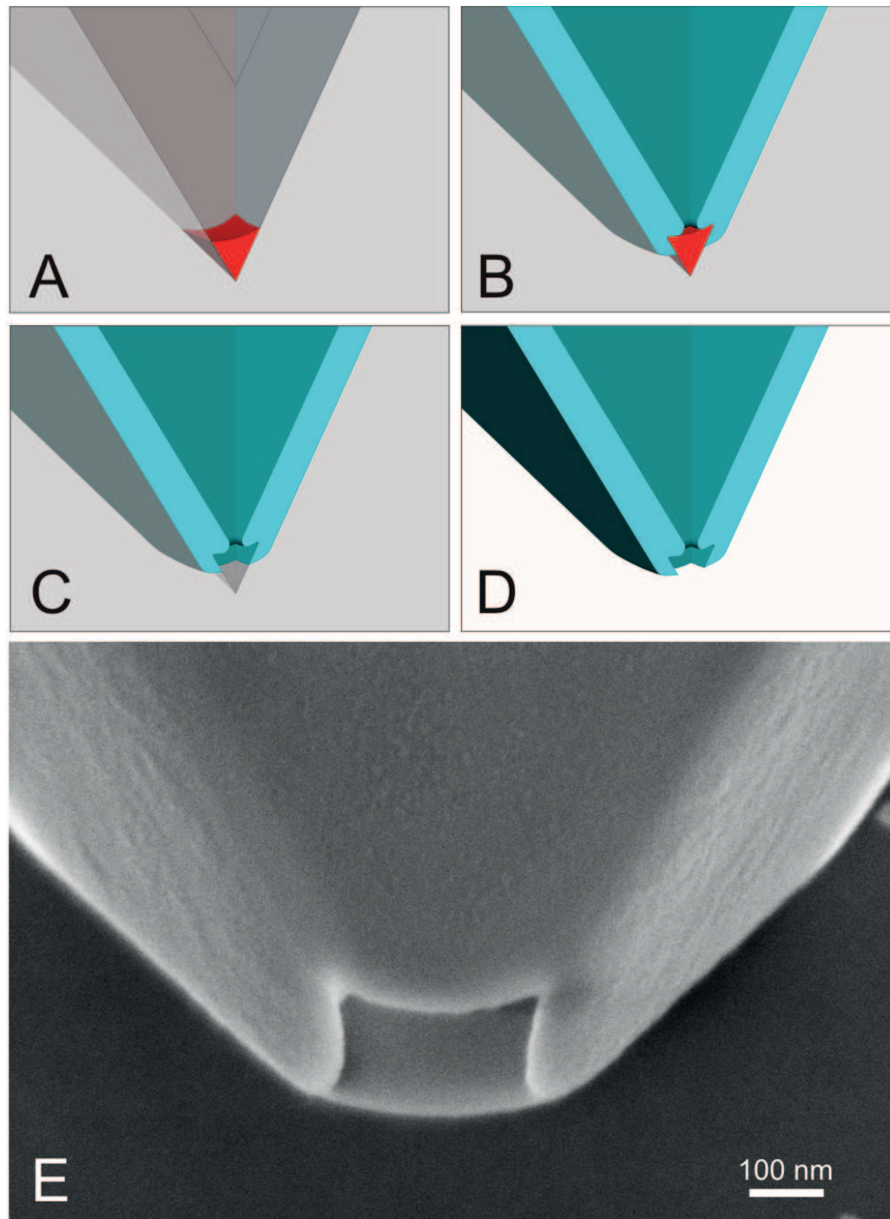


Figure 3.2: Fabrication scheme for aperture at the apex of the pyramid. A) Conformal deposition and isotropic thinning of silicon nitride, B) LOCOS, C) Selective removal of the silicon nitride inversion mask, D) Removal of the silicon mold, and E) Resulting aperture (approx. 240 nm across).

free the aperture. Figure 3.2 illustrates the main steps and shows a SEM photograph of a typical result. The process flow starts by forming an inverted pyramidal mold by anisotropic etching using a square mask opening in a $< 100 >$ silicon wafer. Next, a layer of silicon nitride is conformally deposited by low-pressure chemical vapor deposition (LPCVD) as the first step of the corner lithography. Based on the angle of the corners, this will result in a thickness $1/2t\sqrt{6} \approx 1.22t$ in the apex ($\alpha = 70.6°$) of the pyramid and $1/2t\sqrt{6} \approx 1.22t$ in the ribs ($\alpha = 109.4°$) (Burouni et al., 2011). Here t denotes the thickness of the silicon nitride at the flat surface. In the subsequent isotropic etching step (in HF solution), an etch distance between t and 1.22t results in a nanowire pyramid (Sarajlic et al., 2005), while a distance between 1.22t and 1.73t results in a nano-dot as is needed here (Figure 3.2A). These steps constitute the corner lithography.

To create the freestanding pyramid containing the aperture, the next step is local oxidation of the silicon (LOCOS) using the nitride dot in the apex of the pyramid as a mask (Figure 3.2B), selective removal of the silicon nitride dot in phosphoric acid (Figure 3.2C), and finally selective removal of the silicon mold (Figure 3.2D). Figure 3.2E shows a fabricated aperture (diameter of approx. 240 nm) based on a deposited silicon nitride layer of 340 nm, a silicon oxide layer of 110 nm (on the $< 111 >$-planes), and an etch factor of 1.35 (etch distance 1.35t). The etch factor has been chosen sufficiently above the lower limit of 1.22 to anticipate for possible wafer scale non-uniformities. A detailed study on the issue of uniformity of corner lithography will be reported elsewhere. It shows that non-uniformities in the silicon nitride deposition and etching for a layer thickness as in the current experiment is in the order of 5% (Burouni et al., 2011). The effective etch factor therefore can vary between 1.30 and 1.40, leading to small variations in the aperture size. The size of the resulting aperture is approximately 240 nm (measured from side to side). This is in reasonable correspondence with the size of the silicon nitride dot, based on the initial layer thickness of 340 nm and an ideal corner lithography process with an etch factor of 1.35 ± 0.05. Under these assumptions the top width of the nitride dot is 200 ± 20 nm. To give an indication of the realized uniformity, we measured the aperture size across an area of $3 \times 1cm^2$. In general the apertures can be slightly rectangular due to the fact that the original mask opening for making the mold is not a perfect square. For the smallest side we measured an average of 203 nm with a standard deviation (SD) of 33 nm. For the largest side we measured 230 nm with a SD of 61 nm. This larger SD is caused by the fact that the mask imperfection has a random character.

Using the corner lithography approach it is expected that sub-100 nm apertures can be reached by reducing the initial silicon nitride and silicon

oxide layer thicknesses. It is at this point important to compare our approach with the wafer scale techniques presented before Mihalcea et al. (2000) created a silicon oxide pyramidal structure in an anisotropic etch pit in a silicon mold. The combination of the oxidation retardation in the apex and an HF thinning step (when the pyramid is still in the mold) leads to a reduced thickness of the silicon oxide near the apex of a silicon oxide pyramidal structure. The apertures are opened when the mold is removed (in a KOH wet etch). The resolution of this technique is limited by the fact that the thinnest oxide is formed near and not at the apex. The smallest aperture size reported was 80 nm. Minh et al. (1999) introduced a method where a silicon oxide pyramid is opened at the apex by thinning down the oxide at the convex side of the pyramid, so after removal of the mold. Important in this thinning step is the protection of the inside of the pyramid by a metal layer. This method yielded apertures as small as 25 nm. An important difference of these two reported methods with the corner lithography method is that the aperture is formed while the mold has already been removed. In corner lithography the aperture is formed while the structure is still in the mold, which allows for further processing of the structure formed.

Controllable Apertures at the Side of a Pyramid

The aim of this experiment was to create a pyramid with apertures close to the tip. Fabrication starts with KOH etching to form a pyramidal mold in a $< 100 >$ silicon wafer. Next, LPCVD silicon nitride structural material is conformally deposited, followed by LPCVD poly silicon which will act as an etching mask in later steps. A second layer of silicon nitride was conformally deposited and isotropically etched in HF to form a dot in the tip apex (corner lithography, Figure 3.3A). This remnant serves as an inversion mask in the LOCOS step (wet oxidation) of the polysilicon (Figure 3.3B). After removal of the silicon nitride dot, a timed retraction etching of the polysilicon follows, from the apex of the pyramid moving upward (see arrows, Figure 3.3C). The duration of this step determines the height of the side-apertures to be formed.

In the performed experiment, a layer of 330 nm polysilicon etched laterally at a speed of 420 nm/min. in a 5wt% TMAH solution at 70.6°C. Next the silicon oxide is removed and the free accessible first silicon nitride etched in H_3PO_4. This also is a timed etch step (etch factor 1.04) as it should leave the four silicon nitride nanowires and the tip (Figure 3.3D). Figure 3.3E shows a typical fabrication result with apertures of about 1.8 μ in height. The size and the location of the side-apertures can be tuned by the thickness of in particular the silicon nitride layers (485 nm for the first layer and 120 nm for

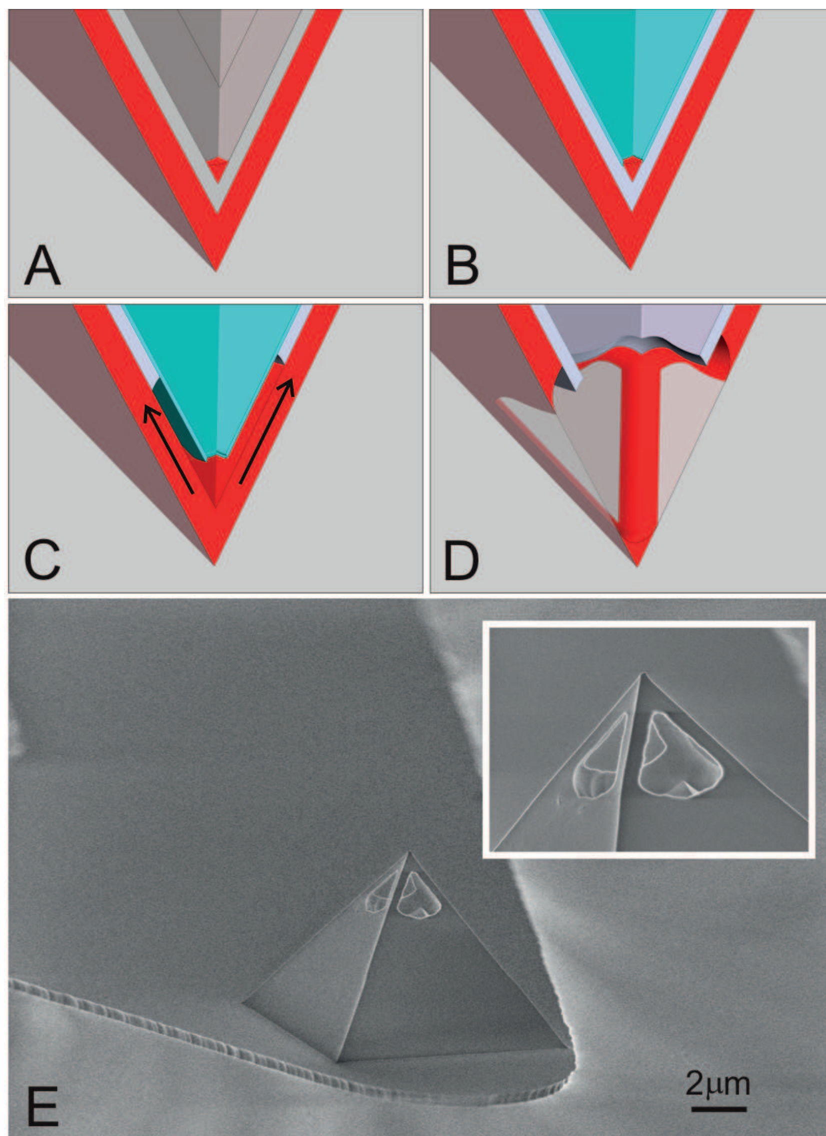


Figure 3.3: Fabrication of side-apertures (A-D). A) Deposition of silicon nitride, polysilicon and second silicon nitride layer. Corner lithography applied to second silicon nitride. B) LOCOS applied to the poly silicon layer. C) Removal of silicon nitride dot and subsequent retraction etching of the poly silicon. D) Removal of the silicon oxide mask, subsequent corner lithography of the first silicon nitride layer. E) Fabricated silicon nitride tip containing the side-apertures, suspended on a cantilever beam.

the second layer in the current experiment) and by the poly silicon etching time (105 s in the current experiment). The cantilever beam is formed in step D using the poly silicon layer as the etch mask.

To test the functionality of the side-apertures, we placed a cantilever carrying a closed pyramidal surface and a cantilever carrying a pyramid with side-apertures close to each other on a piece of clean and smooth silicon wafer. Permanent adhesion (stiction) occurs between the cantilever and wafer surfaces, keeping the pyramids in contact with the substrate (Figure 3.4A, 3.4D). This substrate was then placed in the ESEM. Relative humidity (RH) level was gradually increased from 60% to 100% and SEM images from both tips made at intermediate RH levels. At the specific magnification used in the experiment we could observe a meniscus at RH levels of 95% and above. At 95% RH the meniscus size was still small and did not reach the level of the side-apertures (Figure 3.4B, E). At 96 and 98% the meniscus was grown to a size to reach the level of the side-apertures and a clear confinement effect could be observed (Figure 3.4C, F). Figure 3.4G shows the measured diameter of the neck of the meniscus (indicated by arrows in Figure 3.4C), as a function of RH. We plotted the diameter versus $-1/\ln(\frac{p}{p_s})$ in which p is the water vapor pressure and p_s is the saturated vapor pressure. Following the Kelvin equation, a linear relationship is found for the closed pyramids when we assume that p_s =6.47 Torr. This is very close to the tabulated p_s =6.55 Torr for $T = 5°C$ and can reflect a small calibration error in either the temperature or the pressure sensor in the ESEM. As expected there is no significant difference in the measured diameter between the closed pyramids and the pyramids having side apertures for 95% RH. For 98% RH (the right two points in Figure 3.4G the effect of the side-apertures on the diameter of the capillary neck can be clearly be observed. This experiment shows the potential for controlling the size of the meniscus by nano-structuring of the pyramidal tip, which is for example important in nano-deposition techniques like fountain pen lithography and NADIS. However, it is only a first step as these techniques also need a guiding path for the ink from the base of the pyramid to the tip apex.

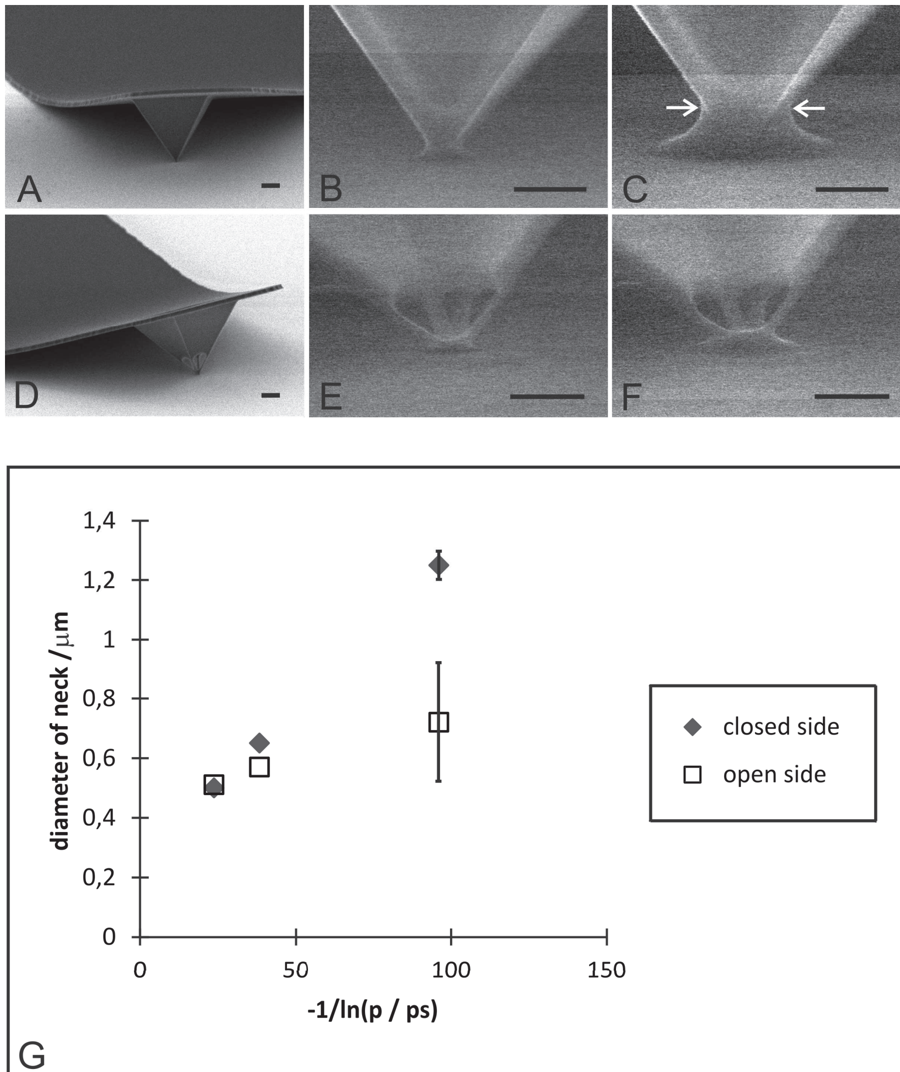


Figure 3.4: A solid (A), and a pyramid containing side-apertures (D) was brought in contact with a substrate (oxidized silicon wafer) by adhesion of the supporting cantilevers to the smooth substrate. B), E) ESEM photographs of the meniscus forming at the solid and perforated pyramid (95% RH), and C), F) at 98% RH. A confinement effect can be observed due to the presence of the side-apertures. The scale bars represent a 1 μm distance. Quantitatively, the graph (G) shows the measured diameter of the capillary neck for the solid pyramids (diamonds) and the pyramids having side apertures (squares). The deviation from the linear trend due to the confinement effect of the windows at 98% RH is significant. The error bars are indicative for the min-max errors in "closed side" neck diameters (small error), and the "open side" neck diameters (large error).

3.2.2 Nanowire Trapping Device

When the over-etch factor in corner lithography is in the range of 1.0 - 1.22, nanowires will remain in the ribs of a pyramidal mold, etched in a $< 100 >$ silicon substrate (Sarajlic et al., 2005). Here, we integrate this pyramidal nanowire structure in a complete microfluidic filter device and demonstrate its basic functionality. Figure 3.5A-D illustrates the main fabrication steps. A silicon nitride layer is deposited and etched using a regular photoresist pattern of 5 μm diameter holes. The thus formed micro-patterned nitride layer is used as an etch-mask in the formation of the inverted pyramidal mold structures in silicon (wet anistropic etching in TMAH). To create the nanowire pyramid, silicon nitride is conformally deposited by LPCVD and isotropically etched in H_3PO_4 solution. In the present experiment an etch factor of 1.05 was applied. To create a fluidic interface, glass tubes (3 mm id) are fusion bonded to the membrane by melting the glass at $790°C$ (Moğulkoç et al., 2009; Unnikrishnan et al., 2009a).

Figure 3.5E shows a SEM photograph of the multi-scale assembly. To test the functionality of the trapping device it was placed in a transparent reservoir filled with DI water, on top of an inverted microscope. Approximately 5μL of bead suspension (4.5 μm diameter latex microspheres, polybead ®, Polysciences) equivalent with 1.5×10^5 beads was deposited in the glass tube by careful pipetting. Next, 0.2 mL DI water was added to create a water level approximately 1 cm above the level in the reservoir. The created pressure difference was sufficient to induce a flow through the membrane and to force beads into the nanowire pyramids. Figure 3.6A shows optical microscope images taken at 100 s time interval, showing bead trapping events. Figure 3.6B,C show scanning electron microscope (SEM) photographs of trapped beads after drying of the structure. An important parameter is the underetching of the silicon nitride mask layer during the formation of the pyramidal pit. It determines the size of the hole in the membrane with respect to the size of the triangular openings in the wire frame. In the current experiments we used 25 wt% TMAH at $75°C$ to form the pyramidal pits in the silicon mold. This etchant has an etch rate of 16 nm/min in the $< 111 >$ direction.

The device is ideally suited for trapping living cells in a relative open environment, allowing subsequently for techniques like perfusion, electroporation, patch clamping, and fluorescent microcopy. Primary bovine articular chondrocytes were successfully seeded following the procedure of Figure 3.7A. As can be observed in Figure 3.7B-E we were able to obtain a good cell seeding efficiency. In most cases almost all cells could be trapped in the pyramid shaped nanowires. When trying to maximize the seeding density, we obtained about 80% trapping coverage while inserting just enough cells

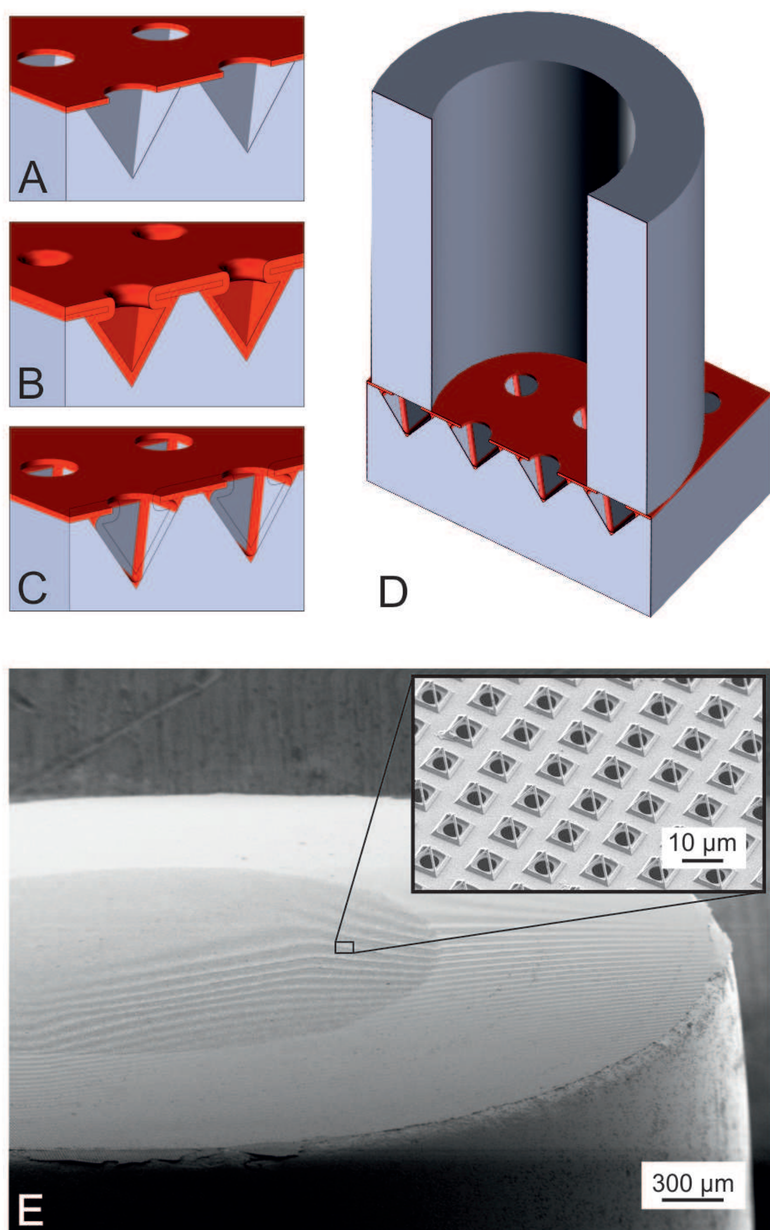


Figure 3.5: Fabrication scheme of nano-wire trapping device. A) Patterning of silicon nitride mask layer and anisotropic etching of inverted pyramids. B) Conformal deposition of structural silicon nitride layer. C) Isotropic back etching of the silicon nitride. D) Fusion bonding of a glass tube for interfacing. E) SEM photo of the resulting structure, looking at the filter membrane.

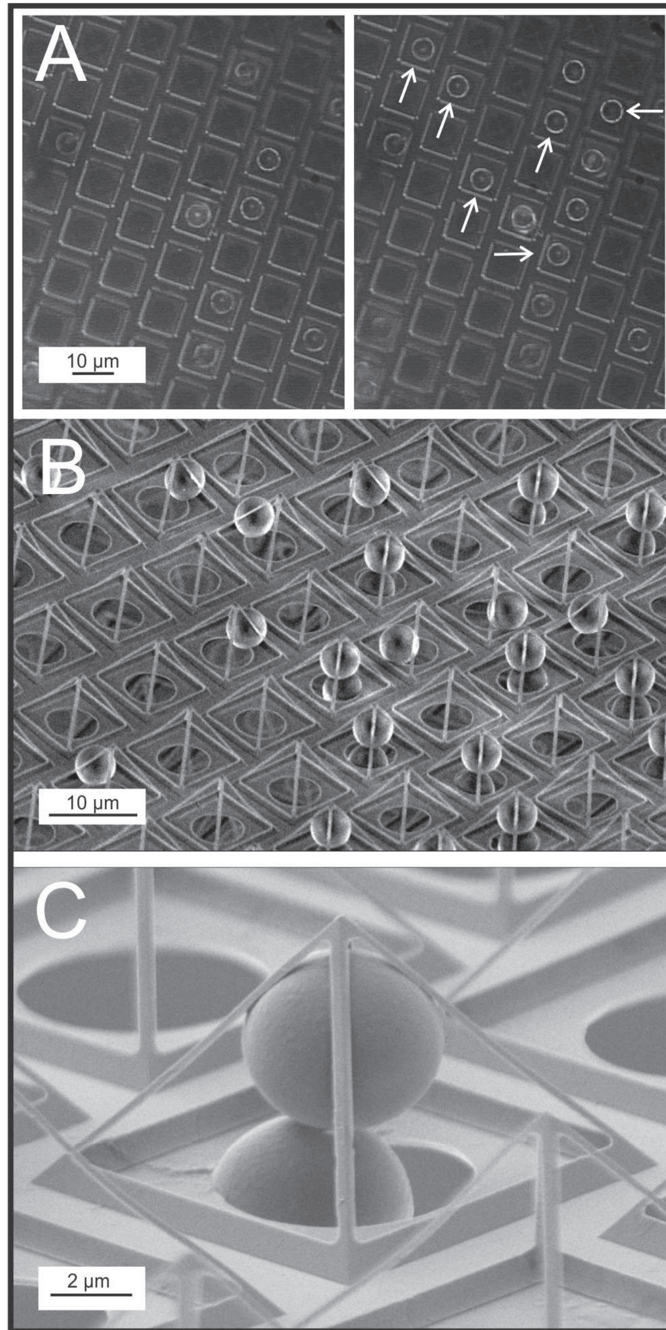


Figure 3.6: A) Optical microscope images of the bead trapping experiments. The arrows indicate the beads there are trapped in the 100 s time intervals. B, C) SEM photographs of trapped beads after drying of the device.

for a theoretical 100% trapping coverage. We usually used a lesser number of cells for seeding than the total number of pyramids present in one array, and then observed that occasionally a few cells were not captured. Subsequently, cells were cultured for up to 48 hours and we observed that they retained a round morphology. Interestingly, within 2 hours after seeding filopodia-like structures could be seen which were anchoring the cells to the pyramids (Figure 3.7C). During prolonged culture these filopodia-like structures increased in quantity and started to bridge between individual pyramids. These fibrous structures resemble extra cellular matrix proteins as described by others during more prolonged cultures in specific tissue engineering studies (Moroni et al., 2008) of chondrocytes for the formation of cartilage. During prolonged culture, individual cells were neatly kept in a predefined pattern and spacing showing that these nanowire arrays can be a feasible tool for studying single cells on a large scale in 2D while maintaining a more natural 3D phenotype.

It is generally known that chondrocytes dedifferentiate into cells with a fibroblast like appearance when cultured on a standard 2D tissue culture plastic surface. Chondrocytes are generally embedded in a vast majority of extra cellular matrix and therefore are generally believed to benefit from a three dimensional environment for retaining their natural chondrocyte phenotype (Cancedda et al., 1995; von der Mark et al., 1977; Buschmann et al., 1992; Bonaventure et al., 1994; Lee et al., 2003). In contrast the pyramid arrays are able to retain chondrocytes with a more rounded phenotype resembling their native phenotype. Several authors have shown the importance of cell shape and attachment for the preservation of, or differentiation into a specific phenotype. Macbeath et al. have shown that if the area a mesenchymal stem cells can adhere to is severely constrained these cells tend to display an adipocyte phenotype, while if these areas are large enough they differentiate into an osteoblast like phenotype (McBeath et al., 2004). The use of 3D corner lithography allows for the creation of 2D cell culture devices containing individual 3D cages for the entrapment of cells in a 3D microenvironment in a controllable and reproducible manner.

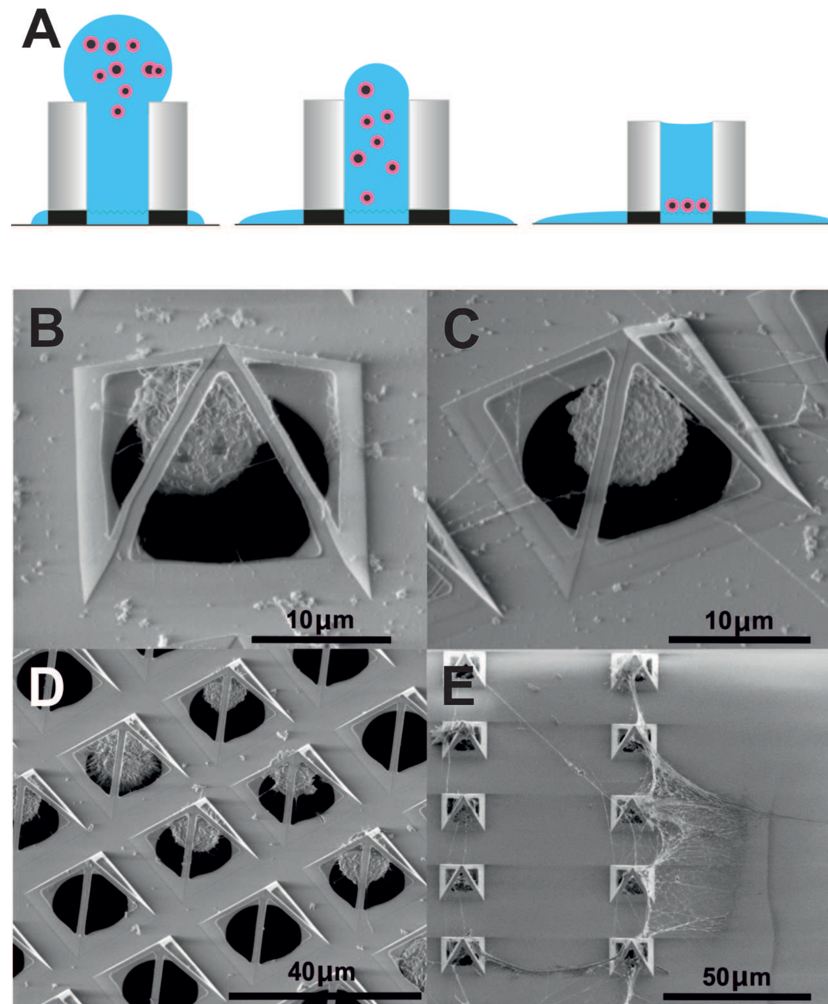


Figure 3.7: Seeding procedure and culturing results. A) Schematic of cell seeding, cells in suspension were added in a droplet on top of the borosilicate tubes after which they settle in individual nanowire pyramids. Flow is induced by a combination of surface tension and gravitational forces. After applying the cell suspension, additional droplets (3-4) of cell culture medium maintains the downward flow directing individual cells into the pyramids. B) Primary bovine chondrocytes 1 hour and C) 2 hours after seeding. Chondrocytes can be seen adhering to the ribs of the pyramid shaped nanowires while maintaining their rounded morphology. D) 24 and E) 48 hours after seeding filopodia-like structures and protrusions can be seen extending through, and bridging in between the cages.

3.3 Conclusions

In conclusion we demonstrated the batch-wise fabrication of sub-micron features (apertures and wires) by a new 3D nano-patterning technique and their

integration into functional fluidic devices. We demonstrated the basic functionality of the side-apertures in confining the water meniscus grown in the contact zone of the pyramidal tip. Arrays of nanowire pyramids were successfully integrated in a complete microfluidic filter device, and the trapping of micro-beads was demonstrated. Individual bovine primary chondrocytes were successfully cultured in an array of pyramids, while retaining a 3D morphology comparable to their native phenotype. In addition, we observed filopodia-like structures and protein-like deposits produced by these cells suggesting the onset of ECM formation starting already 2 hours after initial cell seeding. Future work will focus on using the tool to study behavior of several different primary cell types and the influence of nanowire pyramid cultures on (stem) cell differentiation and adhesion. In device fabrication we will work on further downscaling of the corner lithography. We will expand the use of the technique in making functional nanostructures in other domains, such as thermal, mechanical, and magnetic domains.

3.4 Experimental Section

Nano-aperture fabrication: First a 100 nm silicon oxide mask layer is grown by wet thermal oxidation at $900°C$. A mask pattern containing $5 \times 5 \mu m^2$ squares was applied by standard photolithography. After patterning the mask layer in buffered HF solution, a 1% HF dip was applied for 1 minute to remove native oxide just before wet etching of the silicon. Pyramidal pits were etched into the silicon by KOH solution (25 wt%, at $75°C$) for 15 minutes. Samples were cleaned in RCA2 solution (HCl:H_2O_2:H_2O = 1:1:5, $80°C$) and HNO_3. A 1% HF dip (1 minute) was applied to remove native oxide prior to depositing a conformal low stress film of silicon-rich silicon nitride (SiRN) layer of 340 nm by LPCVD (200 mTorr, $850°C$, SiH_2Cl_2 : NH_3 flow = 3: 1). The SiRN layer was etched isotropically in H_3PO_4 solution (85 wt%, $180°C$) for 102 minutes to remove a thickness of 1.35 times the deposited layer thickness. This leaves a dot of approx. 200 nm across in the apex of the pyramid. The exact etch rate was checked using a dummy wafer containing the same deposited thickness of SiRN.

An inversion step was carried out by LOCOS using the silicon nitride dot as the inversion mask (30 min. wet oxidation at $950°C$), resulting in a silicon oxide layer of 110 nm (on the $< 111 >$- planes). To open the aperture at the apex the SiRN dots were removed in H_3PO_4 solution (36 minutes) after a 1 minute HF etching step (1% HF) to remove the silicon oxi-nitride formed in the LOCOS step. These steps are done in presence of a dummy wafer to check the annealed SiRN etch rate (the etch rate in H_3PO_4 is typically 30%

reduced after the oxidation step). Finally, to release the pyramids the wafer was broken and the silicon etched from the side for 20 minutes in a TMAH solution (25 wt%, at 75°C).

Side-aperture fabrication: A 120 nm SiRN-layer was deposited on a 100 mm $< 100 >$ silicon wafer using LPCVD and patterned by reactive ion etching (RIE, Electrotech, Plasmafab 310-340) using a resist mask with 5 μm holes and the following etch parameters: 10°C electrode temp., 25 sccm CHF_3 flow, 5 sccm O_2 flow, 10 mTorr pressure, 75 W power. After stripping the photoresist, pyramidal holes were etched in a KOH solution (25 wt%, 75°C) after which the wafer was cleaned in RCA solution. Tip sharpening of the mold was achieved by wet oxidation of the silicon mold (at 1000°C) after stripping the silicon nitride mask in 50% HF for 45 minutes. To create the structure in Figure 3.3A a layer of 500 nm silicon nitride, a layer of 330 nm poly silicon and a layer of 120 silicon nitride were subsequently deposited by LPCVD (an HF dip proceeding the last deposition step).

Corner lithography was performed to the last layer using HF 50% (3.6 nm/min etch rate). An etch factor of 1.27 was used, calibrated by etching of a dummy wafer in parallel. Inversion of the created dot in the apex was achieved by local oxidation of the poly silicon (LOCOS) (wet oxidation at 900°C for 10 minutes, approx. 50 nm). To create the cantilever, the LOCOS oxide is patterned by standard photo-lithography followed by 150 s (buffered) BHF etching and stripping of the photo resist. This LOCOS mask is later transferred into the underlying poly silicon and then into the first silicon nitride. To open the poly silicon at the tip apex, the remaining silicon nitride is removed in H_3PO_4 solution (85 wt%, 180°C). To reach to the situation of Figure 3.3C the poly silicon is etched for 105 s in a 5% TMAH solution (70°C), at a lateral etch rate of 486 nm/min (plain layer 700 nm/min). Finally, the LOCOS layer was stripped in BHF, to reveal the poly silicon mask for patterning of the remaining silicon nitride layer (500 nm). Patterning was done by H_3PO_4 etching (85 wt%, 180°C) for 127 minutes (etch factor 1.04) to reach to the situation of Figure 3.3D. The devices were completed by removing the poly silicon mask in 5% TMAH solution (70°C) after an HF dip and anodic bonding of the silicon wafer to a pre-diced pyrex wafer (450°C, 800 V). Prior to bonding an 8 nm LPCVD oxide layer was deposited to avoid bubble formation during anodic bonding. After dicing from the backside of the glass wafer the silicon nitride devices were etched free by KOH etching (25 wt% at 70°C for 8 hours) followed by RCA cleaning and stripping of the sharpening silicon oxide in BHF for 7 minutes. This completed the devices up to the stage that they can be released by breaking -out the samples.

ESEM experiments: A cantilever carrying a solid pyramid and a can-

tilever carrying a pyramid having side-apertures were placed close to each other on a piece of clean and smooth silicon wafer. Permanent adhesion (stiction) occurs between the cantilever and wafer surfaces, keeping the pyramids in contact with the substrate. The substrate was then placed in the ESEM (FEI/Philips XL30 Feg). Experiments were carried out at a fixed chuck temperature of $5°C$. The relative humidity (RH) was regulated by varying the water vapor pressure from 3.9 to 6.4 Torr in six steps, corresponding with RH levels increasing from 60% to 98%. At each RH level an ESEM image was taken from both tips at the same magnification.

Nanowire trapping device fabrication: A 500 nm silicon-rich silicon nitride layer (SiRN) is deposited on a 100 mm $< 100 >$ silicon wafer using Low-Pressure Chemical Vapor Deposition (LPCVD) and patterned by reactive ion etching (RIE) using a resist mask with 5 μm holes. After stripping the resist in an oxygen plasma and native oxide removal by 1%HF, pyramidal pits bounded by $< 111 >$ planes are etched through these holes in 25% TMAH at 75°. (Etchrate $< 100 >$ planes = 300 nm/min, etchrate $< 111 >$ planes = 16 nm/min). Etching time of 97 min. gives an undercut of the SiRN mask holes of 1.9 μm. Next, the structures are conformally coated by a LPCVD SiRN layer of 770 nm $+/-$ 20 nm followed by isotropically thinning down in 85% H3PO4 at 180° leaving the nanowires in sharp concave corners. Tuning of the etching time is based on etching SiRN dummy wafers having the same thickness as the process wafers. Ellipsometric measurements (plasmos SD 2002 ellipsometer) in combination with hydrophobic surface change sets the endpoint of etching the SiRN. An over-etch factor of 1.05 was applied for compensating the non-uniformity of the SiN layer ensuring wafer scale nanowire fabrication.

Backside removal of 500 nm SiRN is done using RIE (first deposited SiRN layer). Borosilicate glass tubes (3 mm id, 6 mm od, Duran, Schott AG) are diced at 20 mm length and polished to optical grade. They are fusion bonded to the membrane by melting the glass tubes at $790°C$ (30 min, ramp-up $10°C$/min , ramp-down $20°C$/min, oven: Nabertherm LH 15/12). Finally, the membrane and nanowires are released by dissolving the silicon substrate wafer in a TMAH solution (5% at $75°C$, etchrate $< 100 >$ planes = 600 nm/min).

Bead trapping experiments: The trapping device was placed in a transparent reservoir filled with de-ionized (DI) water, on top of an inverted microscope (Leica DMI5000). The device was resting on a spacer ring and the membrane just submerged in the water. Approximately 5μL of bead suspension (4.5 μm diameter latex microspheres, polybead ®, Polysciences) equivalent with 1.5×10^5 beads was deposited in the glass tube by careful pipetting. Next, 0.2 mL DI water was added to create a water level approxi-

mately 1 cm above the level in the reservoir. The created pressure difference was sufficient to induce a flow through the membrane and to force beads into the nanowire pyramids. During the experiment the membrane was observed in bright field mode, through a 40x objective (HCX PL Fluotar, NA 0.60 (Corr.)). Trapping experiments were continuously recorded by a camera (Procilica CV 1280), at a frame rate of 10 images per second.

Cell culture and seeding single cells: The initial nanowire trapping device was adapted to allow for cell entrapment and tissue culture handling. In brief the dimensions were adapted to allow for the seeding of primary bovine articular chondrocytes, (passage 3, p3). Nanowire trapping devices with a pore diameter of 16 μm and membrane rib width of 19.6 μm and 10.7 μm height were produced according to the previously mentioned micromachining method. Cryopreserved primary chondrocytes (p2) were thawed and plated at 3000 cell/cm^2 and cultured until 80% confluence during 6 days at 37°C, 5% CO_2 using DMEM (Gibco-BRL, the Netherlands) supplemented with 10% fetal bovine serum (Sigma-Aldrich, Milwaukee, WI, USA), ascorbic acid 2-phospate (0.2 mM, Gibco-BRL, the Netherlands), non-essential amino acids (0.1mM, Sigma-Aldrich, the Netherlands), proline (0.4 mM, Sigma-Aldrich, the Netherlands), penicillin (100 units/ml, Gibco-BRL, the Netherlands) and streptomycin (100 mg/ml, Gibco-Brl, the Netherlands).

Subsequently cells were washed 2x in PBS and trypsinized and resuspened in PBS to a final stock solution of 50 cells/μL. Cells were seeded in droplets of 20 μL deposited onto a borosilicate tube, which was bonded on top of the nanowire trapping array according to the schematic in Figure 3.7 and using droplets of 20 - 30 μL. After applying the cell suspension, additional droplets (3-4) of cell culture medium maintains the downward flow directing individual cells into the pyramids. Cells were allowed to settle and attach for 2 hrs, and subsequently cultured for 24 hrs and 48 hrs. Cells were fixed afterwards using 4% paraformaldehyde and dehydrated using an increasing ethanol solution series (70 to 100%). Samples were then processed for SEM using a Balzers-CPD030 critical point dryer and gold sputter coated using a Cressington 108SE sputter coater and observed using SEM (FEI Quanta 450).

Chapter 4

Pyramidal Nanowire Tips for Atomic Force Microscopy and Thermal Imaging

4.1 Introduction

Atomic force microscopy and Scanning thermal microscopy (SThM) (Edinger et al., 2001; Piner et al., 1999; Mills et al., 1998) are widely applied techniques for the study of nanoscale phenomena. At the heart of the SThM technique is a modified scanning probe, which has a sharp tip with a nanowire cross junction integrated at its apex. Such a probe can be realized by crafting a AFM cantilever using direct deposition of platinum by focused electron beam (Edinger et al., 2001). However, this fabrication method is rather impractical and time consuming. Another approach is based on micromachining and multiple level direct-write electron beam lithography (Piner et al., 1999; Mills et al., 1998; Chong et al., 2001). The high cost of an E-beam system and the serial nature of its writing process make this method both expensive and unsuitable for high-volume manufacturing. We present a scanning microscopy probe for AFM and thermal imaging fabricated by standard micromachining and conventional optical contact lithography.

Thermal probes can be used in two ways, either with temperature feedback, also called active mode, or without temperature feedback, called passive mode. The passive mode is the constant current mode; a small constant current is applied to the probe, in this way the probes works as a thermometer. The active mode is a constant temperature mode; the temperature feedback keeps the probe at a constant elevated temperature by heating the thermal element. The way this is done depends on the method used. For the resistive wire this is achieved by resistive joule heating. When a probe comes near a sample, heat flows between the tip and the sample, depending on

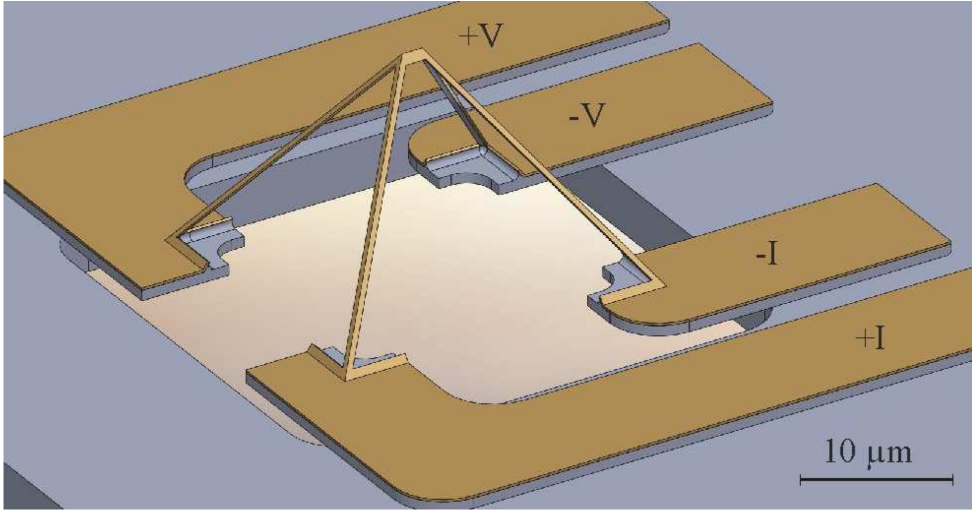


Figure 4.1: Schematic illustration of a silicon nitride wireframe tip, coated with conducting layer to enable thermal imaging.

the difference in temperature. The power delivered to the tip to keep it at constant temperature is a measure for the local temperature and/or thermal conductivity of the sample (Gmelin et al., 1998; Hammiche et al., 1996). A Scanning Thermal Microscope (SThM) can be used in Atomic Force Microscopes (AFM) and Scanning Tunneling Microscopes (STM). In this way both topography and thermal properties can be investigated simultaneously. The advantage of using an AFM is that insulators as well as conductors can be examined. We apply a recently discovered nano-fabrication technique (Burouni et al., 2011; Berenschot et al., 2008; Sarajlic et al., 2005) to develop sophisticated probes with electronic functionality for scanning probe microscopy. This method, called corner lithography, can be used to realize three-dimensional wireframes with nanometer diameters, using simple micrometer scale optical lithography. This method is inexpensive and can be applied on a wafer scale, is perfectly suited for small scale production and is compatible with conventional micromachining. The probe, shown in Figure 4.1, features an AFM-type cantilever with a pyramidal tip composed of four freestanding silicon nitride nanowires. The nanowires, which are made of silicon nitride coated by metal, form an electrical cross junction at the apex of the tip, addressable through the electrodes integrated on the cantilever. The cross junction on the tip apex can be utilized to produce heat and detect local temperature changes and perform AFM and thermal imaging by scanning the probe tip over a surface.

4.2 Fabrication

4.2.1 Corner Lithography

Corner lithography method results a well size-controlled fabrication procedure for well-defined nanometer scale structures with exact position and spatial arrangement fully determined by the template. We employed this technique to define uniform nanowires. Corner lithography is based on the material that is left in sharp concave corners after conformal deposition and isotropic etching (Figure 4.2). Controlling the size of remaining material l, which is depends to the angle of the corner α and initial thickness t, is related on the etching time with respect to the removal layer during etching r.

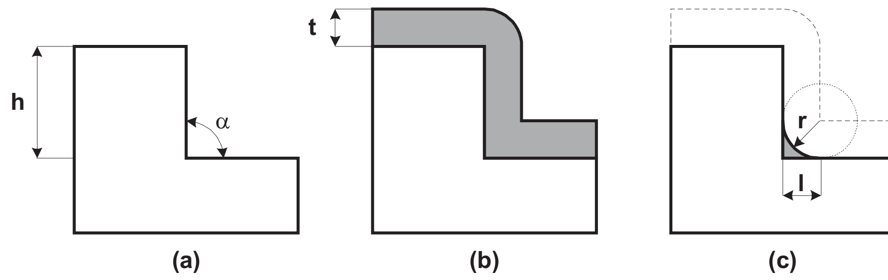


Figure 4.2: Principle of corner lithography: exploiting conformal deposition and isotropic etching.

4.2.2 Pyramidal Nanowire Tip

We have successfully fabricated a first probe prototype with a nanowire tip composed of approximately 60 nm width and 11 μm long silicon nitride wires metalized by 6 nm Ti and 35 nm Au layers as shown in Figure 4.3 (Sarajlic et al., 2010). To fabricate nanowires with approximately 60 nm width, first a 192 nm low stress silicon nitride was deposited. Then, the layer was overetched for 10% of initial thickness to have 60nm width as result (Figure 4.4). Consequently, the radius of the tip r will be 211 nm at the end.

The corner lithography technique leads to highly uniform wires. Figure 4.5 shows the standard deviation of the silicon nitride layer as a function of etching time. This standard deviation results in an uniformity of the over etch factor of 1.1±0.04.

To be able to use this nanowire pyramid in applications such as SThM and SHPM a conductive layer has to be applied on the pyramid and the leads.

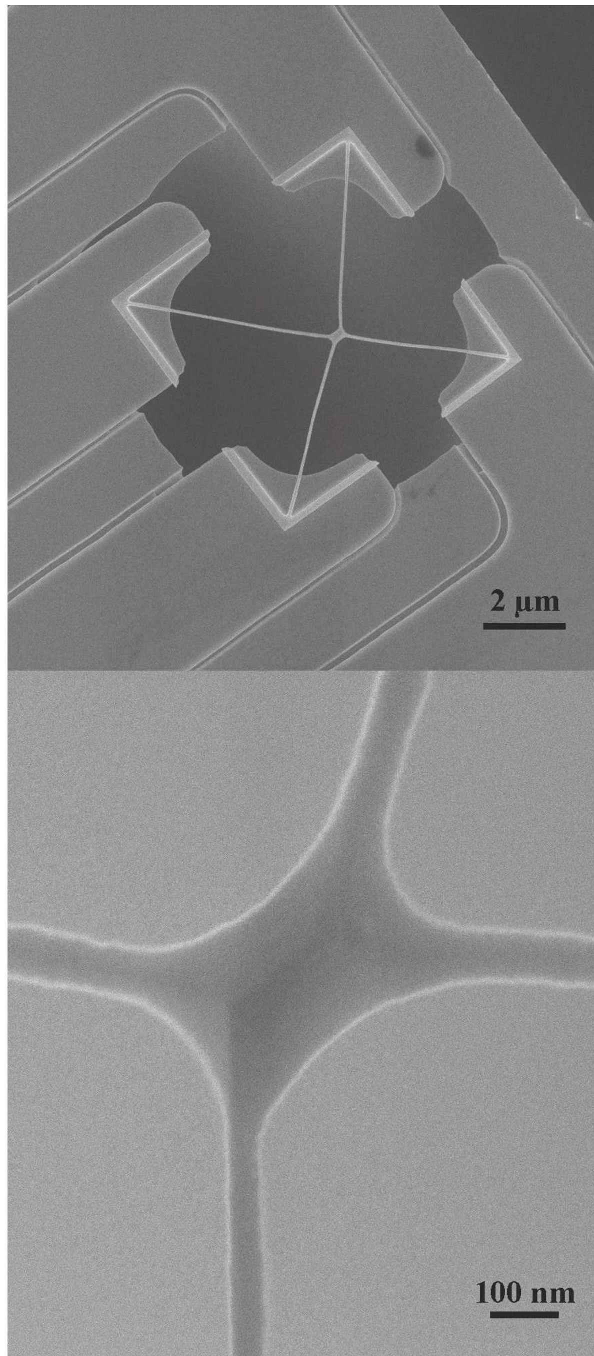


Figure 4.3: HRSEM images of the fabricated probe. Top: overview of the wire-frame and electrodes. Bottom: tip apex. The wire width is approximately 60 nm. The wires are coated with a Ti(6 nm)/Au(35 nm) layer.

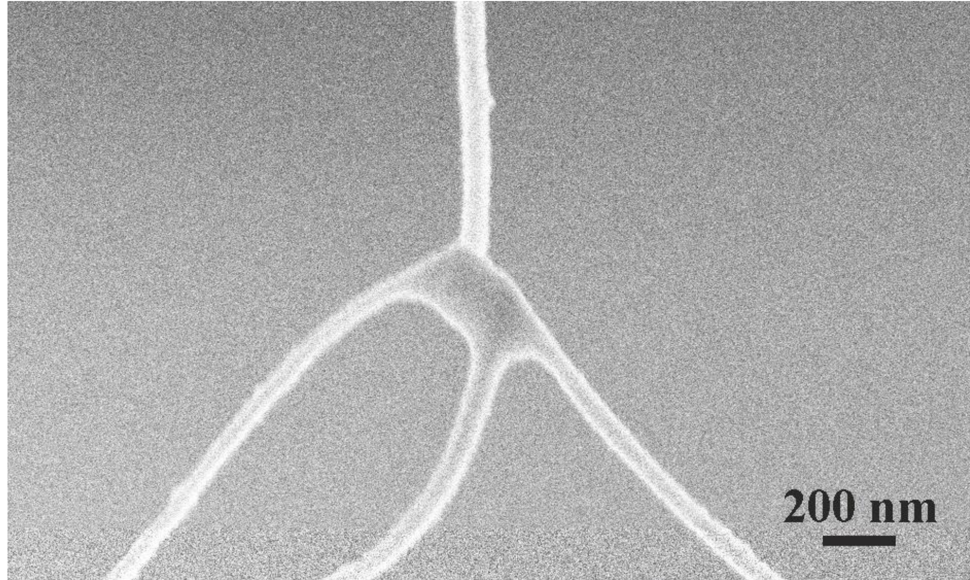


Figure 4.4: Side view of the tip apex. The inner radius is around 211 nm.

For this a sputtering process with a titanium bonding layer and a gold layer is used. In this way a resistive nanowire tip is created. The conduction through the metal layers on the cantilever and the nanowires is mainly determined by the gold layer, as it has a thickness in the order of 35 nm or more, and the thickness of the titanium layer is less than 10 nm, and the resistivity of titanium is approximately 20 times higher than the resistivity of gold.

4.3 Results

4.3.1 Electrical and Thermal Properties

When a constant current runs through the nanowires, the entire wire heats up. The uniform heat power delivered to the nanowires is V^2/RL , where V is the voltage applied to one pair of the nanowires and R is the resistance and L is the length of the nanowire. The temperature distribution reaches a steady-state after heating in fraction of second. This gives an indication that steady-state heat transfer can assumed. The electrical resistance of the nanowires forming the pyramidal tip is a function of temperature. In order to demonstrate the temperature dependence, we have resistively heated the tip by passing a DC current through one pair of nanowires. For each measurement point (V and R), the current is kept constant until the resistance stabilizes.

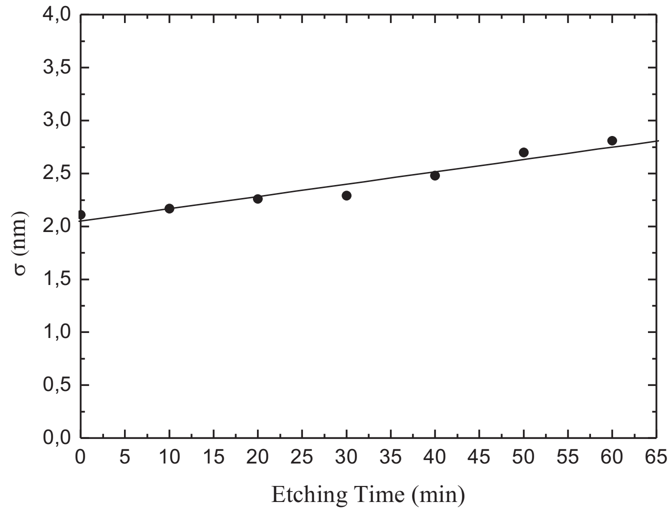


Figure 4.5: Standard deviation of the silicon nitride layer during etching by 50% HF in wafer scale which is related to the initial thickness of the nitride, etching time and number of the measurements in each point.

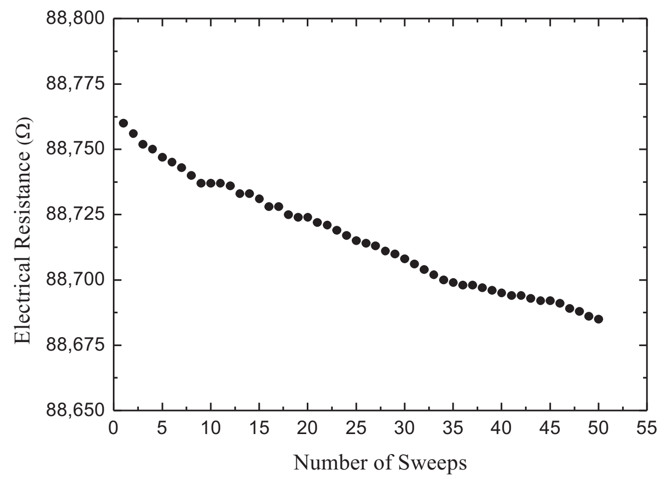


Figure 4.6: Electrical resistance of the nanowires when sweeping the current from 0 up to 0.5 mA.

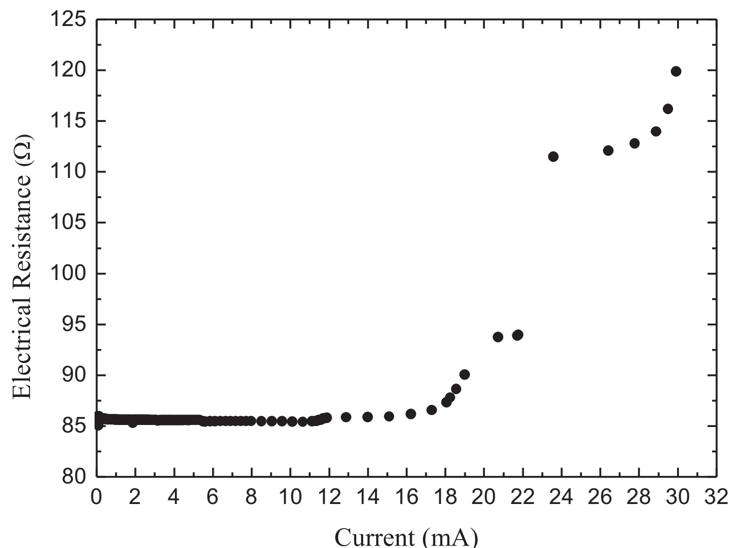


Figure 4.7: Electrical resistance of the wire as a function of current. In each measured point, current is kept constant until resistance stabilizes.

The change in electrical conductance to other nanowire pair induced by the heating of the tip was measured using lock-in techniques (Figure 4.1). The resistance was around 89 Ω which fits well with 119 Ω as theoretical expected resistance. By sweeping the current, the resistance decreases and can be described as a function of the number of sweeps as shown in Figure 4.6. Sweeping the current improves the electric conductance through the probe. After a current sweep the wire resistance slightly decreases (see Figure 4.6). A possible explanation is that the current heats the bottlenecks in the gold layer, which have the highest resistance, enough to cause the gold layer to become somewhat more mobile and in that way reorder the gold atoms in and around those points. This decreases the resistance of those points, resulting in a decrease of the overall resistance.

The temperature changes in the nanowires due to Joule heating can be sensed by measuring the resistance of the nanowires. It is expected that temperature changes of a surface can be sensed in the same way. The current through the nanowires can be expected to be limited by a maximum current density because this is the most limiting factor of the lifetime of the wire, and not the temperature. Electro migration will destroy the wire before Joule heating does Pierce and Brusius (1997). In Figure 4.7, as expected,

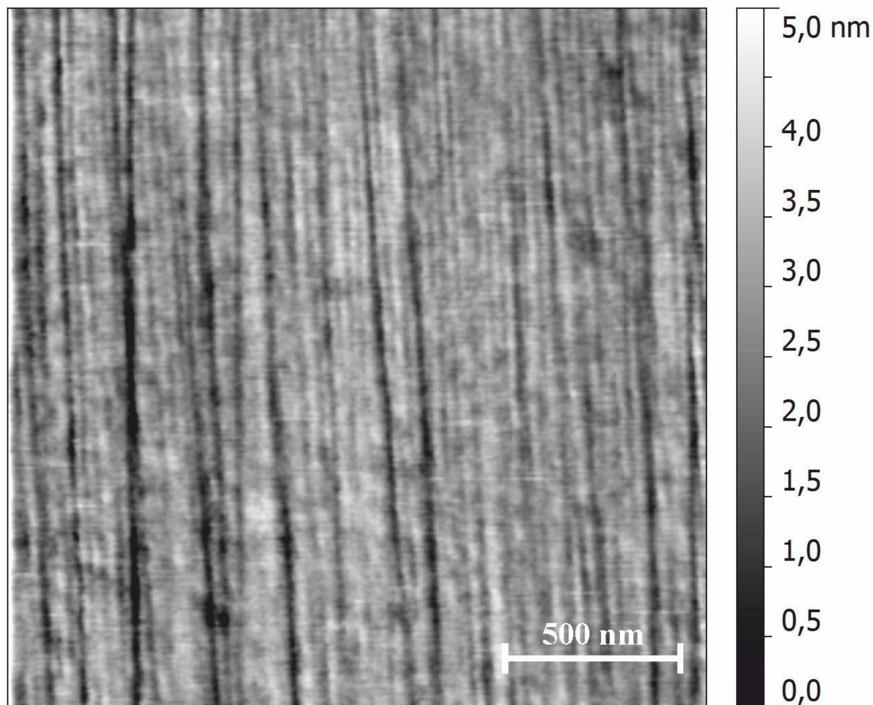


Figure 4.8: AFM scan of a magnetic hard disk surface, using a sharp wireframe probe.

the electrical resistance increases with increasing the heating current from 11 to 18 mA. At a current of 18 mA, we estimate the maximum temperature to be [390 K], based on the temperature coefficient of thin film gold (0.0017 K^{-1} (Zhang et al., 2007)). Above 18 mA we suspect that electromigration occurs.

4.3.2 Atomic Force Microscopy

We employed the scanning probe in an atomic force microscope. Figure 4.8 shows a contact AFM scan of a magnetic hard disk taken with a sharp pyramidal wireframe probe. The resolution is higher than the tip outer dimensions, most likely since we scan with only one corner. The probe was scanned many times on the surface of the sample without damaging either the sample or the tip.

4.4 Conclusions

We present a novel wireframe probe for atomic force and scanning thermal microscopy, based on corner lithography. The batch fabrication process results in silicon nitride wires with approximately 60 nm width and a standard deviation as low as 2-3 nm. These nanowires are coated with a 41 nm Cr/Au layer. The wires can be heated by means of an electrical current. From the increase in resistance with current, we estimated the maximum temperature to be 390 K at a current of 18 mA. When sweeping the current several times from 0 to 0.5 mA, we observed a non-reversible reduction in the resistance of about 15 ppm per sweep. The probes work well in tapping mode AFM, and we observed a resolution of 50 nm when scanning the surface of a magnetic hard disk. These results give us confidence that these exiting new probes can be successfully applied in scanning thermal microscopy, to either measure the thermal conductance or temperature of surfaces.

Chapter 5

3D Nanofabrication of Self Aligned Sub-30 nm Aperture and Nanowires by Repeated Corner Lithography

5.1 Introduction

There has been a significant increased demand for the fabrication of smaller three-dimensional (3D) nanostructures leading the aim of developing versatile, rapid, accurate, wafer-scale and low-cost fabrication methods. There are several constraints with the current methods that limit the exploration, research and development of 3D nanostructured devices such as nano mechanical systems (Waggoner and Craighead, 2007), nanophotonics (Soukoulis and Wegener, 2011), and nanofluidic devices (Xia et al., 2012). In practice, real devices are three-dimensional and are mostly generated by multi-layer structuring during their fabrication process. Several approaches have been developed to use multi-layer structure and layer-by-layer methods. Some of these methods are to design the characteristic of the fabrication process based on the desired structures, which comprise holography (Campbell et al., 2000), self-assembly (Vlasov et al., 2001), directional etching (Takahashi et al., 2009), performing different acceleration voltages in electron beam lithography (Tanenbaum et al., 2001; Boyd and Blaikie, 2006; Matsubara et al., 2006), or multiple exposure (Vila-Comamala et al., 2011). In practice, very large limitations can be mentioned for these approaches such as massive patterning restrictions, mostly on the periodicity or repeatation of structures. Moreover, the number of layers is limited. These approaches may not be used versatilely in the process of 3D nanofabrication.

In addition to the custom design methods, there are more general approaches that can be used to fabricate several types of structures that need particular equipment. They consist of direct laser writing (Deubel et al., 2004), nanomanipulation (Tandaechanurat et al., 2011), wafer bonding (Noda et al., 2000), and membrane stacking (England et al., 2012; Patel and Smith, 2007). A more developed method can be addressed as the direct laser writing that uses multi photon absorption technique. This method has the advantage of rapid patterning the prototypes, but achieving high resolutions can be a tough challenge (Ledermann et al., 2006). Even though several developments have been done to improve the resolution in the methods with diffraction limitation (Fischer and Wegener, 2011; Sakellari et al., 2012), the improvements are limited. It has been shown that low resolution of the photoresist and the polymer scaffolds cannot be used in elevated temperatures due to their low temperature resistance (Liou and Pretzer, 1998).

There are several steps in conventional layer-by-layer methods to reach 3D nanofabrication of devices, which are complicated and have limitations with adaptation with other material platforms. To achieve ultra-high resolutions, electron-beam lithography technique can be used, but it is not cost effective. Prototyping of 3D nanostructures with multilayer hydrogen silsesquioxane (HSQ) scaffolds can be performed faster with lower costs with high resolution and temperature, but miniaturization and reaching sub-100 nm scales can be a restriction (Varghese et al., 2013).

Corner lithography is a method to fabricate 3D nanostructures smaller than resolution of photolithography (Burouni et al., 2011, 2013; Berenschot et al., 2012; Sarajlic et al., 2005; Burouni et al., 2011). This method is compatible with scaling down the size of the nanostructure, which agrees with the primary design size expectations. It is a low cost and fast method which is accurate, uniform and the whole process can be controlled for wafer-scale manufacturing on a substrate with uniform size and properties (Sarajlic et al., 2005). It needs template with sharp concave corners that can be used for conformal deposition of the first material. In the next step, the first layer is isotropically etched and another material is deposited and the primary material is then removed. The remaining material in corners can be used as mask material or as structural material.

This method can be used to fabricate 3D nano-apertures (Burouni et al., 2011, 2013), 3D nanowires, and silicon oxide pyramids containing nanoscale metal tips (Berenschot et al., 2012; Sarajlic et al., 2005; Burouni et al., 2011). It can be employed to fabricate a conductive nanowire, which is applicable in Scanning Thermal Microscopy (SThM), and as thermal sensor. 3D tip fabrication with different designs for SPM such as moveable SERS probe, fountain tip (Berenschot et al., 2012) and atomic force microscopic (AFM)

probe (Burouni et al., 2011), are other corner lithography applications (Yu et al., 2009). Even though it is possible to achieve very small nano structured devices (below 50 nm) using single corner lithography method, these devices can be fragile (Burouni et al., 2011).

To create a mechanically stable part which is connected to a delicate thin feature, we introduce the repeated corner lithography (RCL) method (Figure 5.1). It can be applied to fabricate wafer scale, uniform, accurate, and miniaturized nano devices. This method shows a high mechanical stability of structures due to step by step build-up the nanostructure on the residual as base. For example in aperture applications, a pyramidal oxide base is defined with an appropriate thickness that satisfies the design size. Then, the method can be repeated to scale down the size and to reach the desired aperture size.

In this chapter we address the important challenge of how to obtain a small aperture size and thin nanowires constructs, while maintaining the mechanical stability of the pyramidal base structure.

5.2 Results and Discussions

5.2.1 Base Pyramid Fabrication

The first corner lithography step was started with a silicon template with many inverted pyramids having sharp concave corners formed by KOH etching. Then, a conformal nitride layer was deposited. Based on the angle of the corner and feature sizes, required initial thicknesses were calculated by $\frac{a}{t} = 2\cos(\frac{\alpha}{2}) - 2\sin(\frac{\alpha}{2})\sqrt{(\frac{r}{t})^2 - 1}$, which a is the final width in the apex, t is the deposited layer thickness, α is the angle of corner, and r is the relative isotropic etch distance (Burouni et al., 2013). In order to make two different aperture sizes as first opening, the structures were conformally coated by a Si_3N_4 layer of 324 and 168 nm to make 200 and 100 nm aperture size for devices A and B, respectively. The procedure was followed by isotropically thinning down in 85% H_3PO_4, leaving the nano-dots in sharp concave corners. The etching factor was defined as 1.35 (Burouni et al., 2011, 2013). In this case, all the nanowires in the four oblique ribs of the pyramid were removed by the etchant and a nano-dot was left at the end to use as an inversion mask.

Next, the silicon oxide structural material for the pyramid was formed by local oxidation of silicon (LOCOS) using the Si_3N_4 remnant as the oxidation mask. The inversion nitride mask was removed by 85% H_3PO_4, which has high selectivity of etching nitride in presence of oxide (Burouni et al., 2012a).

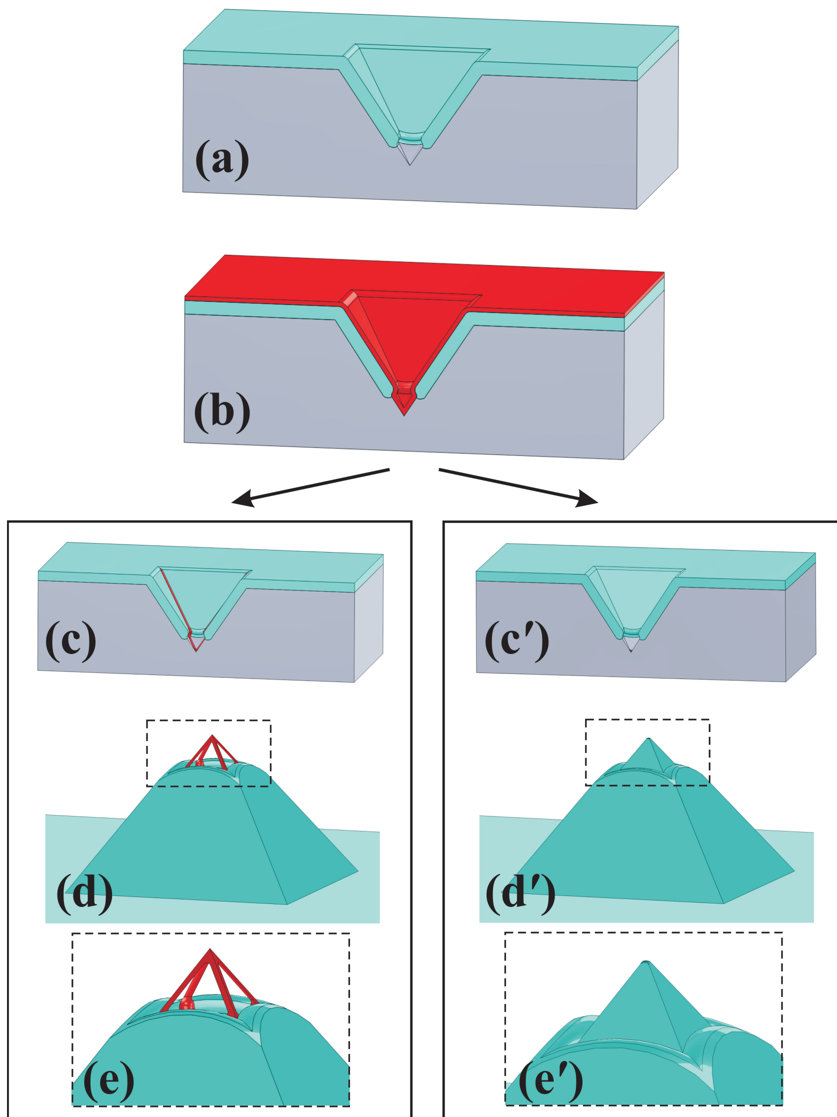


Figure 5.1: A schematic sequence of repeated corner lithography method. The first template is prepared using corner lithography, which is oxide residual with an opening at the apex (a). A thin nitride layer is conformally deposited (b) and isotropically etched ((c) and (c′)). By controlling the etching time, nitride nanowires in the ribs (c) or nano-dot (c′) in the corner with a certain thickness and size are defined. The 3D pyramidal nanowires can be visible by etching back the Si (d and e). The nitride nano-dots can be used as an inversion mask for second LOCOS step. After the second LOCOS, remaining nitride is removed and Si is etched back for better visibility of final tiny aperture (d′ and e′).

Finally, single nano-apertures were fabricated with 200 and 100 nm size for devices A and B, respectively.

5.2.2 Repeated Corner Lithography

Nano-Wireframes on Oxide Pyramid

The sizes of side apertures of the pyramidal nanowires depend on 1) base size, 2) wire thickness (Si_3N_4 thickness) and 3) etching time. The bigger first aperture size results bigger size in four side-apertures in pyramidal nanowires. Therefore, to fabricate 3D nano-wireframes on base oxide pyramid, two different residuals with two different opening sizes were used. Figure 5.2 illustrates the consequence of the fabrication process.

The second corner lithography step has taken place by conformal deposition of 25 nm Si_3N_4 layer to reach sub-29 nm thick nanowires at the end. When the over-etch factor of the layer in corner lithography is in the range of 1.0t to 1.22t, the nanowires will remain in the ribs of a pyramidal mold that is etched in the substrate. The 25 nm of Si_3N_4 layer is isotropically etched regarding the etching factor of 1.00t to result 29 nm nanowires thickness (Burouni et al., 2013). The formed nitride layer is used as an etch-mask in the LOCOS step. Figure 5.3 illustrates the released 3D pyramidal nanowires on top of the oxide pyramids. It can be seen that there is a good correlation between designed fabrication and HRSEM inspection. Figure 5.4 shows the nanowires features from top view, in which the thickness of nanowires in sidewalls can be observed. The oxide has selectively been etched away partly by KOH 25% at 75°C (etch rates: SiO_2=1.6 nm/min, Si_3N_4=0.017 nm/min). These nanowires have been fabricated with 28 nm width, which is in reasonable accordance with the planned 29 nm. Different nanowire thicknesses along the sidewalls to the corner at each ridge are due to different formed angles by silicon or silicon oxide mold in side walls. The angle of the corner of the base pyramid is sharpened due to the LOCOS step.

Nano-Apertures on Oxide Pyramid

In this case, all the nanowires in the four oblique ribs of the pyramid will be removed by the etchant and a small nano dot will be left at the end to be used as an inversion mask (Figure 5.5). To start the second corner lithography, a thin layer of Si_3N_4 was deposited on both A2 and B2 devices (with 200 and 100 nm opening size) and was isotropically thinned down with respect to etching factor of 1.35t. Then, the silicon oxide was gradually grown by local oxidation of the silicon (LOCOS) to form the second pyramidal structure.

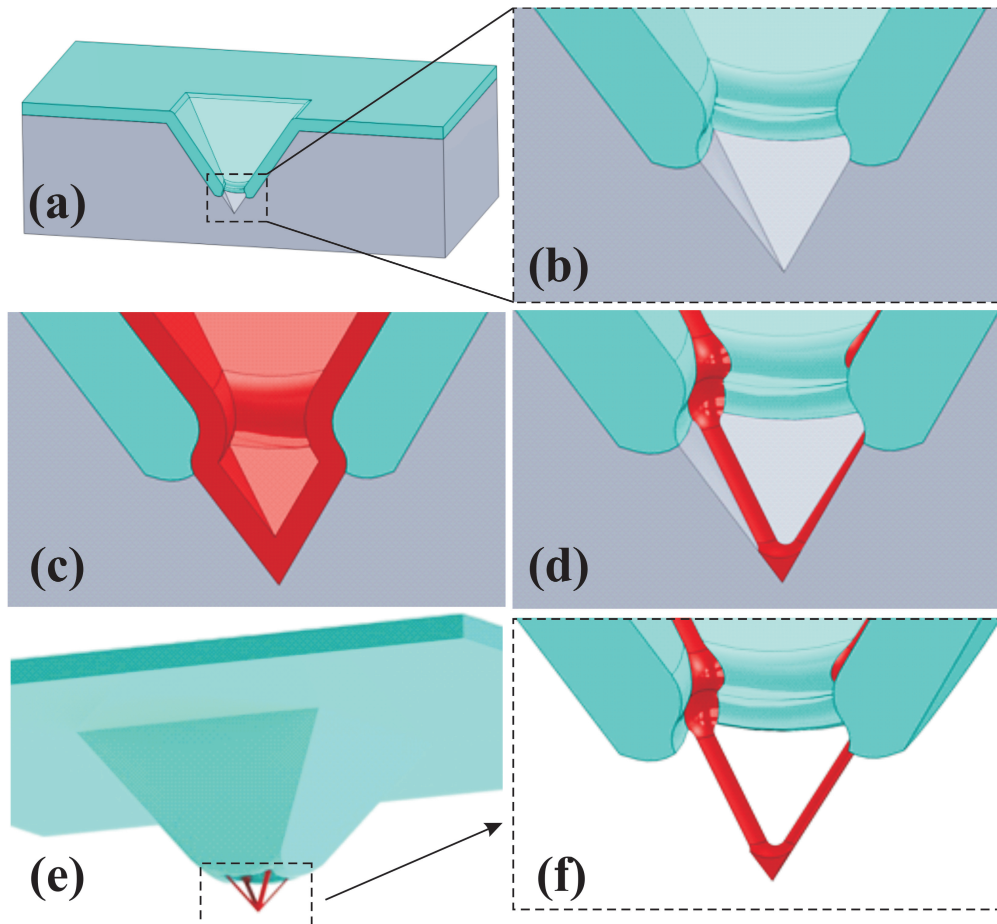


Figure 5.2: Illustration of 3D nanowires on oxide pyramid using repeated corner lithography. To create the nanowire pyramid from the prepared template by corner lithography ((a) and (b)), silicon nitride is conformally deposited (c) and isotropically etched in H_3PO_4 solution (d). By etching back the silicon, 3D pyramidal nanowires are released ((e) and (f)). In the present experiment an etch factor of 1.0t was applied.

Remaining dots at the end of pyramids were removed to make an opening and reach the final aperture at the apex. A schematic process flow is illustrated in Figure 5.5. Moreover, the fabricated sub-30 nm nano-apertures including all components are shown in Figures 5.6 and 5.7.

5.2.3 LOCOS - Temperature and Thickness

The LOCOS process different influences on the opening size in the corner by selecting oxide thickness, oxidation time and temperature and methodology

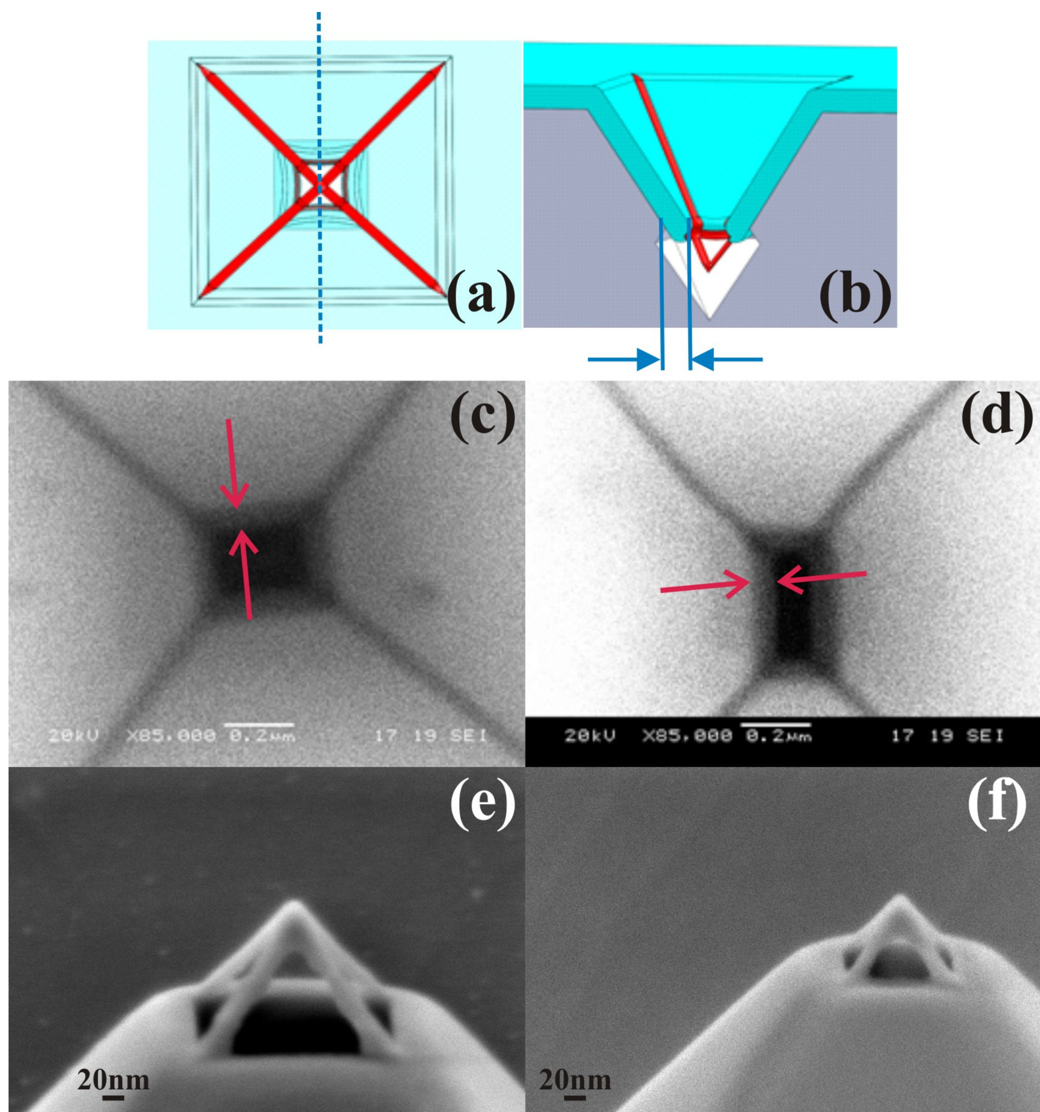


Figure 5.3: Scheme and HRSEM micrographs of nanowires fabricated by repeated corner lithography method. After the first LOCOS step, second deposited nitride layer is partially removed to form nanowires on top of the pyramidal oxide structure, which is shown from top view ((c) for device A1 and (d) for device B1) and in 3D ((e) for device A1 and (f) for device B1). Silicon was dissolved in TMAH to release the structures. The shadow around the aperture is related to the silicon edge in four planes due to TMAH etching ((a) and (b)).

(dry or wet). Therefore, optimization of LOCOS parameters plays a key role at early design stage.

It is known that in silicon oxidation process, the oxide atoms are push-

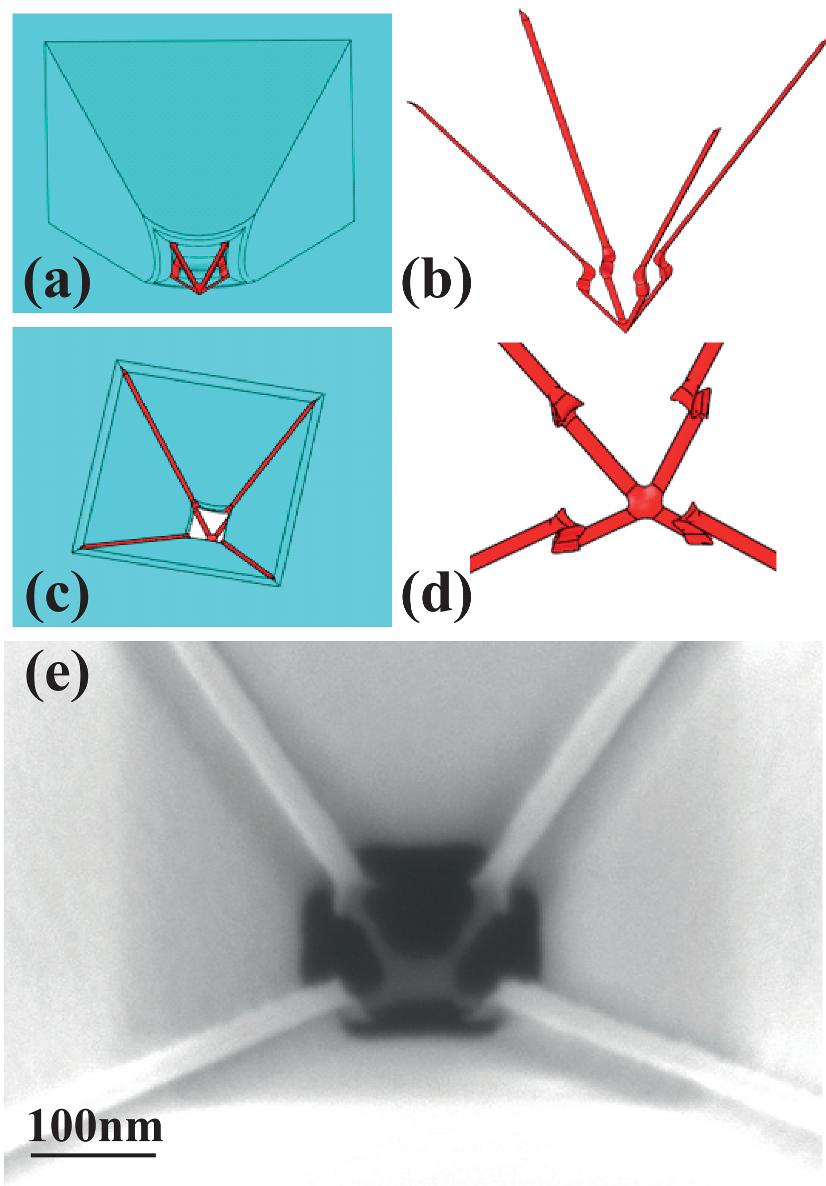


Figure 5.4: Scheme (a-d) and HRSEM micrograph of pyramidal nanowires fabricated by repeated corner lithography from top view (e). Different nanowire thicknesses along the sidewalls to the corner at each ridge are due to different formed angles by silicon or silicon oxide in side walls. The angle of the corner of the base pyramid is sharpened due to the LOCOS step.

ing away the silicon atoms to form the oxide structure and this causes very large internal stresses and more importantly, during ramping down the fur-

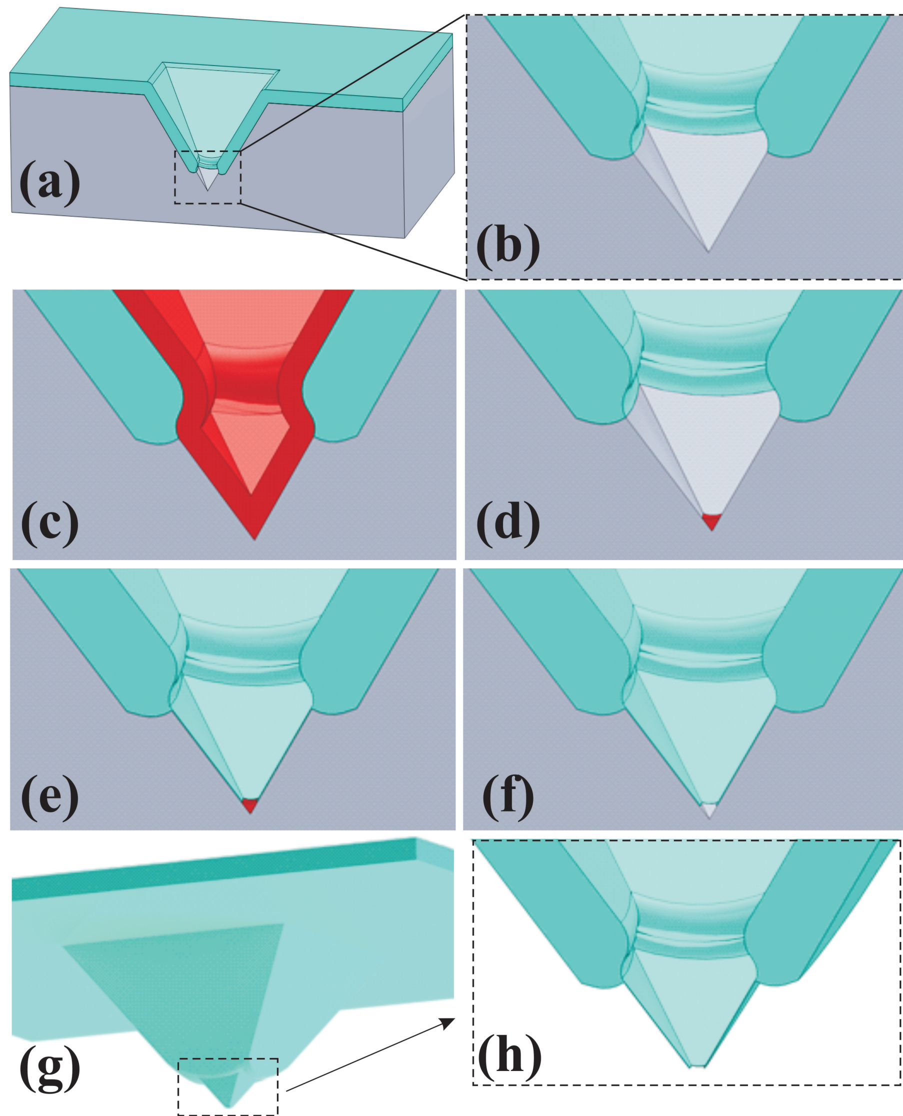


Figure 5.5: A process fabrication of nano-aperture by using repeated corner lithography. To create small aperture from the prepared template by corner lithography ((a) and (b)), silicon nitride is conformally deposited (c) and isotropically etched in H_3PO_4 solution (d). After growing silicon oxide in the second LOCOS step (e), the remaining silicon nitride dot is completely removed (f). By partially etching back the silicon, nano-aperture is released ((g) and (h)). In the present experiment an etch factor of 1.35t was applied.

nace oxidation temperature to room temperature, differences in the material thermal expansion will cause the oxide layer to establish a compressive stress

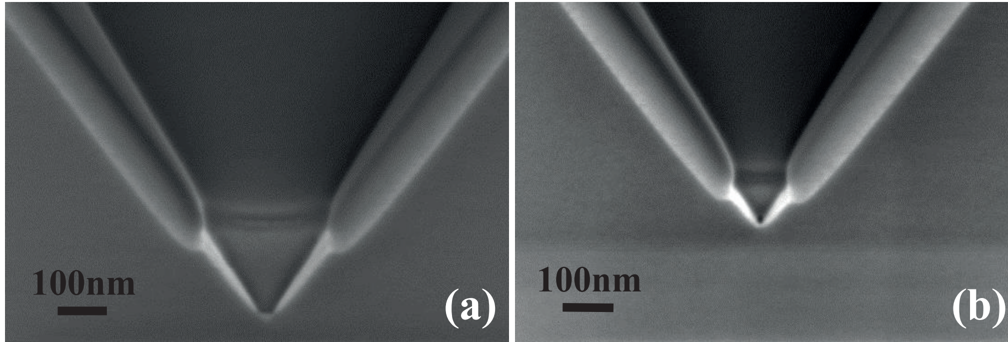


Figure 5.6: Side view of nano-structures fabricated by repeated corner lithography method after the second LOCOS step. Size of the aperture is defined by nitride initial thickness and etch factor, which is related to the etching time. Here the etch factor is 1.35t and designed aperture size is 22 nm.

of around 300 MPa (Jaccodine and Schlegel, 1966; Whelan et al., 1967). The main concerns in design stage are dealing with bird's beak length under the nitride layer in corner and oxide thickness, which have influence on aperture size at the apex and opening size above the nitride dots, accordingly. More importantly, changed in etch rate of nitride after oxidation should be considered. The ideal case is to minimize the length of bird's beak to reach accurate opening size at the end of the process.

The dependence of bird's beak length to wet/dry ambient as well as oxidation time and temperature are known (Kooi and Appels, 1973; Wu et al., 1983). For the same sidewall oxide grown, the bird's beak length under the nitride layer is much shorter with dry oxidation than the wet oxidation. This is because of the high parabolic oxidation rate and therefore, more reaction-limited oxidation process in a wet ambient, which results in a long bird's beak length.

Oxidation at higher temperature gives a shorter bird's beak length since oxidation process becomes more diffusion-limited at higher temperatures. The higher temperature for the LOCOS step gives the lower etch rate for annealed silicon nitride dots. Therefore, removing the dots after the LOCOS step takes longer time, which may affect the thickness of the silicon oxide in sidewalls and opening size as result in the corner. Therefore, tuning the etchant by lowering the temperature for higher selectivity of nitride in presence of oxide is essential (in this work 140°C for phosphoric acid).

The thickness of the nitride mask plays an important role in determination of the LOCOS bird's beak length. From a simple physical point of view, the force required to lift up a beam by a certain distance is proportional to the third power of the beam thickness. Although the oxidation mechanism

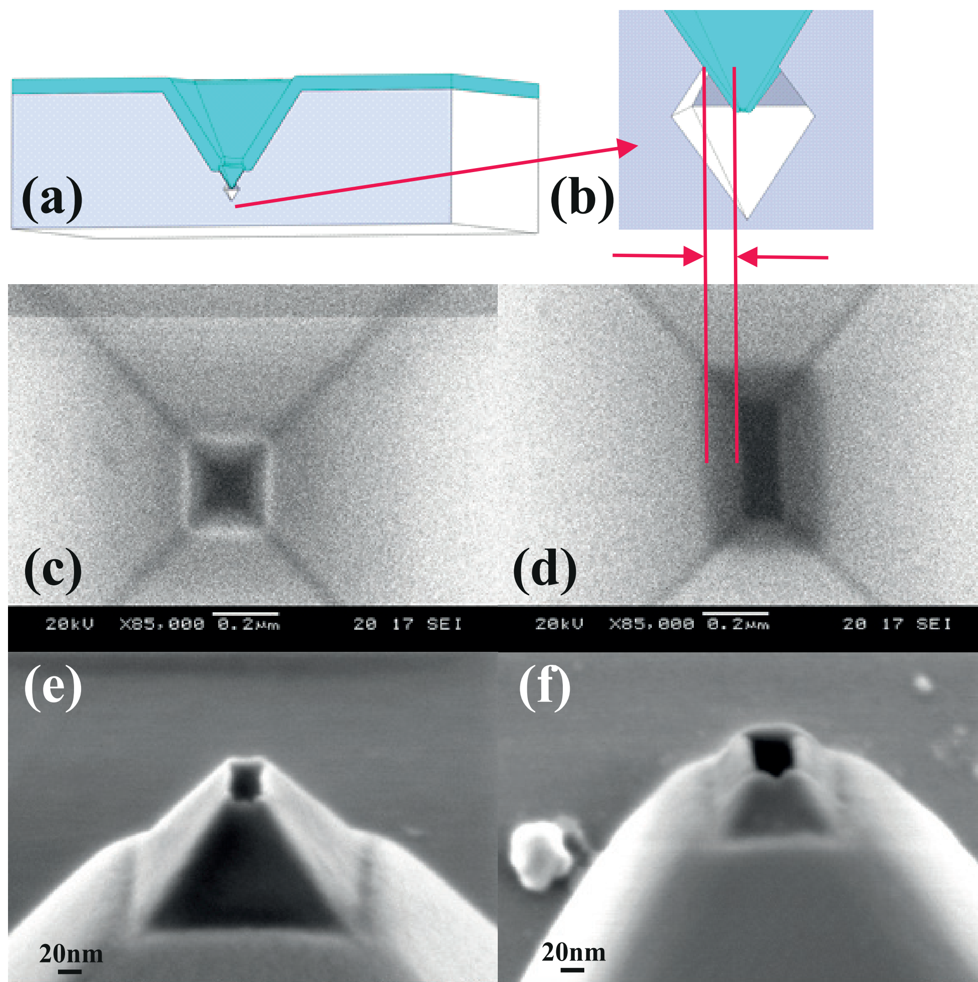


Figure 5.7: Scheme and HRSEM micrographs of the sub-30 nm nano-apertures fabricated by repeated corner lithography method which is shown from top view ((c) for device A2 and (d) for device B2) and in 3D ((e) for device A2 and (f) for device B2). After the second LOCOS step, nano-apertures are achievable by removing the nitride dots at the end with hot phosphoric acid and dissolving silicon with TMAH. The shadow around the aperture is related to the silicon edge in four planes due to TMAH etching ((a) and (b)).

is more complex, the basic concept can still be applied. It is obvious that thicker nitride layers are less prone to bending due to their increased stiffness, which leads to a shorter bird's beak. In our case, the nitride residue is in the concave corners and used as a selective mask to oxidize the unprotected silicon. If the length of the bird's beak is longer than the length of the dots at the apex, the oxide will cover all the structure between the Si and silicon nitride dots. Therefore, aperture will not be opened by removing the nitride

dots after LOCOS step by hot phosphoric acid, which has high selectivity of etching nitride in presence of oxide.

Other concern is oxidation time which the longer leads to grow thicker silicon oxide and it might decrease the size of the opening at the top of the nano-dots in corners and even block the structure. To fabricate nano-structures with mechanical stabilities by corner lithography, a thick layer of the first LOCOS step should be defined. Furthermore, SiO_2 layers in different sidewalls should not meet each other to block the corner on top of the dots. After the LOCOS process, the opening size will be smaller because of the thickness of the silicon oxide (Figure 5.8-a and b). The new size will narrow the space and therefore, has an influence on the etch rate of the annealed silicon nitride dots due to not easily floating the etchant in corners. This effect should be taken into account when timing to remove all the dots to reach the nano-aperture at the apex in the next step. The thickness should be large enough to give a stable structure as result. In addition, it should have enough opening space to deposit second conformal nitride layer to repeat corner lithography without blocking the corner.

By operating at a higher temperature in shorter oxidation period the shorter length of the bird's beak is given (Wu et al., 1983). Experimental results are shown that if the sidewall is grown in a dry ambient and at a higher temperature (tuning oxidation condition in more diffusion-limited kinetics), a much shorter bird's beak length can be achieved (Figure 5.8-c and d).

5.2.4 Oxy-nitride Thickness Estimation

The partial conversion of Si_3N_4 into silicon oxy-nitride (SiN_xO_y) under dry oxidation conditions is known from literature (Fränz and Langheinrich, 1971; Chramova et al., 1981). This transition layer on top of the nitride dots, which is created after the LOCOS step, has high impact on etching time estimation and therefore, nano-aperture size setting due to reach lower etch rate in 85% H_3PO_4 and 1% HF compare to Si_3N_4. Thus, the layer thickness of the transition layer in the oxidation resistance of Si_3N_4 in dry oxidation conditions needs to be found. As an example, the etch plot of a Si_3N_4 layer on dummy wafers in 85% H_3PO_4 after two different dry oxidation run (14 min 22 sec and 36 min 33 sec) at 1050°C show two different trends of etch rates for oxy-nitride and nitride layers (Figure 5.9). Estimation of the oxidation resistance is feasible due to the large increasing in the etch rate in 85% H_3PO_4 as a result of the heterogeneous nature of the layer after oxidation. Ellipsometer measurements on a second substrate were carried out to estimate the thickness of the top oxi-nitride (SiN_xO_y) layer using a two-layer model with the thickness of the core Si_3N_4 and the refractive-indices of Si_3N_4 (n= 2.020)

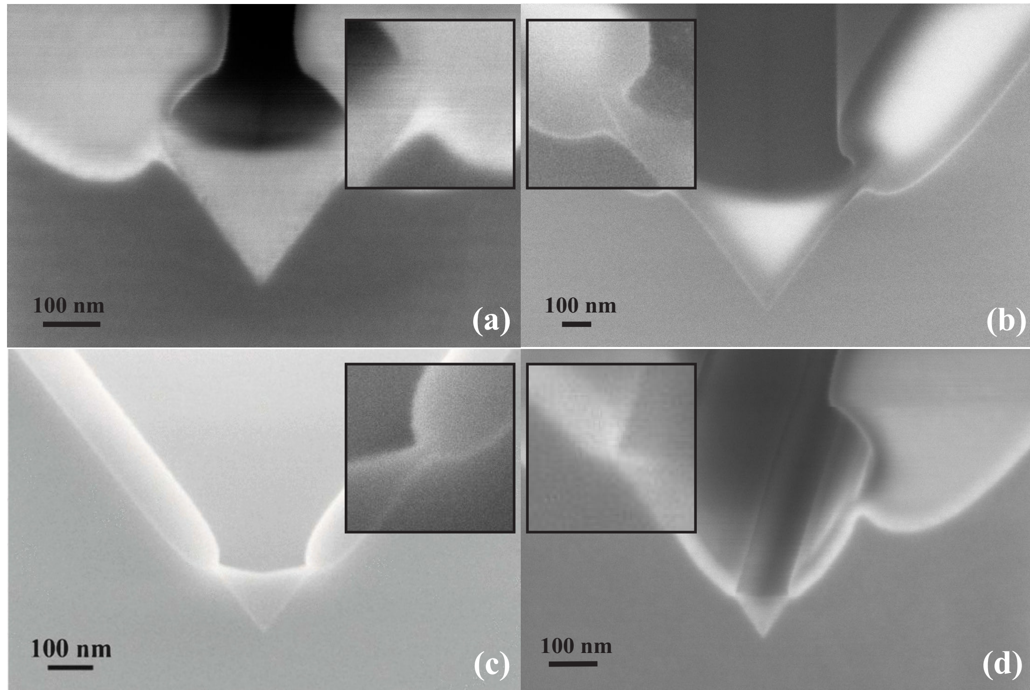


Figure 5.8: HRSEM micrographs of the bird's beak growing (Burouni et al., 2012a) when the nitride is present as a dot with large (a), comparable (b), short (c) and minimum (d) length. After the over etching process, a certain size of the dot remains in the comer. Then, LOCOS step ((a) and (b): wet at 950°C and, (c) and (d): dry oxidation at 1050°C) will form the nano aperture structure in different oxidation times ((a): 41 min, (b): 37 min and, (c): 1 hour 34 min and (d): 13 min for the second LOCOS).

and SiO_2 (n= 1.465) as input parameters. The top layer was found to range from 1.5 nm to 1.6 nm, indicating the lower limit of the thickness of the Si_3N_4 layer to resist oxidation. Previous studies on the material properties have shown that high temperature annealing can cause a strong reduction of the layer porosity by desorption of internal water and structural rearrangements within the thermal SiO_2 layer as shown by infrared spectroscopy (Rojas et al., 1990; Orfescu et al., 1990). The resulting etch selectivity of Si_3N_4 over thermal SiO_2 in 85% H_3PO_4 serves the over etching process condition at higher thermal annealing temperature (in this work 1050°C). The etch rate of SiO_2 in 85% H_3PO_4 was the decisive factor in the engineering process of the present lithographic procedure (corner lithography) to remove oxy-nitride on top of the nitride nano-dots in present of LOCOS layer. It was found to decrease with etchant temperature, but has a high inverse effect on Si_3N_4. Therefore, lowering the temperature of 85% H_3PO_4 gives the higher

selectivity of Si_3N_4 versus thermal SiO_2 (in this work 140°C). As reported in experimental section, the selectivity of Si_3N_4 versus thermal SiO_2 was found as around 16 at 180°C and 24 at 140°C hot phosphoric acid.

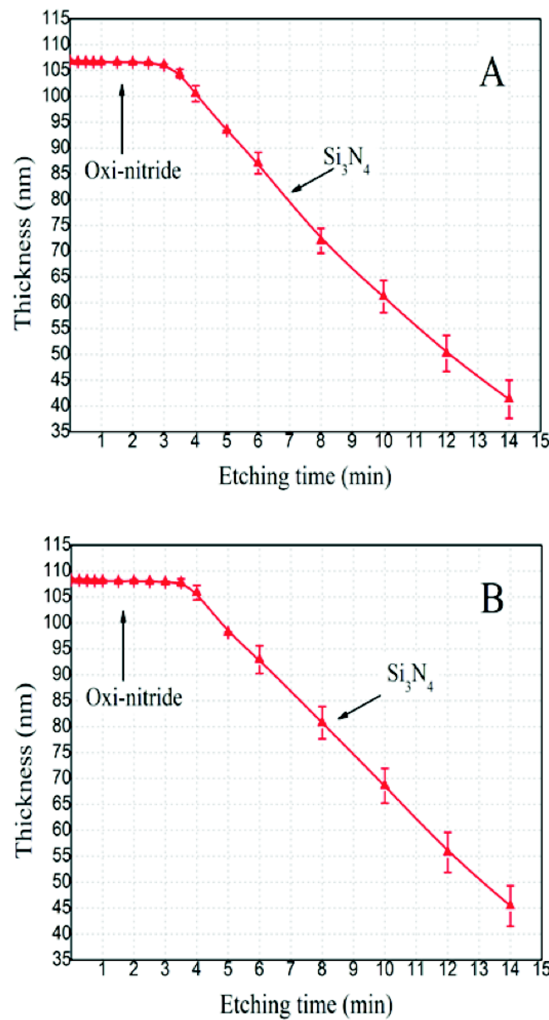


Figure 5.9: Etch rate trend of Si_3N_4 in H_3PO_4 (85% wt, 180°C) after 14 min 22 sec (A) and 36 min 33 sec (B) dry oxidation run at 1050°C. Two different trends in etch rates are obvious due to different etch rate of oxi-nitride and annealed Si_3N_4. The longer oxidation time gives thicker oxi-nitride and therefore, longer time to etch and change the etch rate trend. All data points are measured by ellipsometer.

5.3 Conclusions

We presented a novel method to produce sub-30 nm nano-wires and nano-apertures in three-dimensions on a standard $< 100 >$ silicon wafer. The method used was called repeated corner lithography and offers mechanical stabilities in the structures. This approach could be used in a wide range of micro-electromechanical systems applications that require the fabrication of tips or pyramidal apertures. By repeating the corner lithography, we can obtain small wires/aperture size while maintaining mechanical stability of the structures. Furthermore, the apertures can be employed in AFM based liquid deposition and single cell devices for sequencing purposes.

5.4 Experimental Section

5.4.1 Materials and Tools

All chemicals and materials were purchased from commercial resources: 100 mm OSP $< 100 >$ p-type silicon wafers (Okmatic), Olin 907/12 (Fujifilm Arc), hexamethyldisilazane (HDMS) (100% Selectipur: Merck), OPD 4262 resist developer (Arch Chemicals), HNO_3 (100% Selectipur: Merck, and 69% VLSI: Merck), HF (1% VLSI: Merck), H_3PO_4 (85% VLSI, Merck), and TMAH (75% VLSI: Merck). All experiments were carried out in a cleanroom environment. Layer thicknesses on silicon were determined with Plasmos SD 2002 ellipsometer operating at a wavelength of 632.8 nm. Low-resolution SEM imaging was carried out with a JOEL JSM-5610 SEM operating in secondary electron detection. High-resolution SEM imaging was carried out with a LEO Gemini 1550 FEG-SEM.

5.4.2 Template Preparation

A 70 nm thermal oxide was coated on a 100mm $< 100 >$ silicon wafer. Resist patterns were fabricated on wafers by conventional optical lithography (Electro Visions Group mask aligner (EVG), model EV620) and a periodic hole pattern (circles of 5 μm with 5 μm space) was used as a mask. A dehydration bake on the hotplate (120°C, 5 min) was applied to the wafers before priming with HDMS. Spin coating of the positive photoresist Oline907/12 was done at 4000 rpm for 20 s. A soft bake (95°C, 60 s) was preceding the optical exposure of the resist (3 s, 12 mW/cm, hard contact with 0.7 bar contact pressure) through a mask. After a post-exposure bake at 120°C for 60 s, the resist was developed by mild agitation in OPD 4262 resist developer for 10

min. After patterning SiO_2 layer by BHF etching and stripping the photoresist by 100% HNO_3 for 10 min, 60 s etching by 1% HF was applied in order to remove native oxide layer just before wet Si etching by KOH to create the template. Silicon wet etching was carried out in 25wt% KOH at 75°C. After loading the wafer into the KOH solution, a holding time for etching was set to 6 min. The $< 100 >$ silicon etch rate is about 1.08 μm/min. Afterwards, RCA 2 solution (HCI:H_2O_2:H_2O=1:1:5, 80°C) was applied for properly cleaning the wafers to remove residual potassium ions for 30 min. This gives the final template with inverted pyramids containing sharp concave corners.

5.4.3 Base Pyramid Fabrication

Four prepared templates wafers, 2 for device A (A1 and A2) and 2 for device B (B1 and B2), were chosen to start with. 1% HF was used for 60 s to remove the native oxide layer just before loading the wafers to LPCVD for the first Si_3N_4 layer deposition (LPCVD, Tempress LPCVD furnace: 22 sccm SiH_2Cl_2, 66 sccm NH_3, 800°C, 200 mTorr, 62 min deposition time for device A and 31 min deposition time for device B). These runs were measured using the plasmos ellipsometer and resulted in 324 nm (n=2.008) and 168 nm (n=2.020) for A and B related dummy wafers, respectively. To start nitride wet etching, we employed H_3PO_4 solution (85wt%, 160°C) and dummy wafers to control the etch rate of the Si_3N_4 during over etching process. To remove a thickness of 1.35 times the deposited nitride layer thickness, it was isotropically etched in 85% H_3PO_4 solution at 160°C for 38 min 15 s [113.5 nm (0.35×324) device A] and 21 min [58.8 nm (0.35×168) device B]. The etch rates were 4.0 nm/min and 3.84 nm/min which left a dot with 200 and 100 nm size for A and B, accordingly. After removal of a thin native oxide layer in a 1% HF solution for 30 s, the silicon was oxidized in a dry oxidation furnace (Tempress, dry oxidation furnace, atmospheric pressure, 4000 sccm O_2, 1050°C, 80 min). The measured SiO_2 thickness on $< 111 >$ Si and $< 100 >$ Si were 117 nm and 104 nm (n=1.465), respectively. Remaining dots at the end of pyramids should be etched in presence of dummy wafer to check annealed silicon nitride etch rate. Next, wafers were dipped in 1% HF for 30 s to remove oxide from Si_3N_4, followed by stripping the remaining Si_3N_4 in 85% H_3PO_4 at 140°C. Calculated removal thicknesses were about 320 nm (0.43×324) and 70.5 nm (0.43×164) for 48 min and 24 min, respectively.

5.4.4 Wire-frames on Oxide Pyramid

Devices A1 and B1 (with 200 and 100 nm aperture size on top of oxide pyramid base) were dipped into a 1% HF for 60 s to remove the native

oxide layer just before loading wafers to LPCVD for the second Si_3N_4 layer deposition (LPCVD, Tempress LPCVD furnace: 22 sccm SiH_2Cl_2, 66 sccm NH_3, 800°C, 200 mTorr, 3 min and 45 s deposition time) resulted in 25.71 nm (n=1.938, 3sigma=0.24) and 25.41 nm (n=1.937, 3sigma=0.24) nitride for back and front dummy wafers. Silicon nitride layer was isotropically etched by H_3PO_4 solution (85wt%, 140°C). After loading the wafer into the H_3PO_4 solution (85wt%, 140°C), a holding time used to check etching time (27 min and 9 s). The Si_3N_4 etch rate was about 0.92 nm/min and for SiO_2 0.038 nm/min, both monitored by dummy wafers. Selectivity of silicon over Si_3N_4 was 24. This timing was set to remove a thickness of 1.00 times the deposited nitride layer thickness (25.4 nm). The wafer was broken and the silicon was etched from the side for 10 min in a TMAH solution (25wt%, at 75°C) to partially release the 3D nano-structures.

5.4.5 Nano-Apertures on Oxide Pyramid

The second corner lithography step takes place by conformal deposition of a 35 nm Si_3N_4 layer to reach sub-30 nm aperture at the end. It needs 3 min and 45 s deposition time in LPCVD. Dummy measurement (25 measurement points on one dummy wafer) gave 35.71 nm (n=1.938, 3sigma=0.24) and 35.41 nm (n=1.937, 3sigma=0.24) as results. Similar to the nanowires fabrication steps, H_3PO_4 solution (85wt%, 140°C) and dummy wafers were employed to control the etch rate of the Si_3N_4 layer during over etching process. The nitride layer was etched in 85% H_3PO_4 at 140°C for 51 min and 43 s. The monitored etch rate of silicon rich nitride measured with help of a dummy wafer was 0.92 nm/min. The second LOCOS was defined at 1050°C by dry oxidation technique for 2 min and 30 s. It resulted 21.11 nm in $< 111 >$ (n=1.465, 3sigma=0.77) and 17.45 nm in $< 100 >$ (n=1.465, 3sigma=0.91) dummies. Then, 30 s dipping in 1% HF was applied to remove oxide between Si and Si_3N_4 layer (wet transport). Remaining dots ($0.43 \times 35 = 15.05$ nm) at the apex were removed by H_3PO_4 solution (85wt%, 140°C) with the etch rate of 0.77 nm/min. Experimental etching time was about 20 min. Thus, the nitride layer was etched in 85% H_3PO_4 up to the end to open nano-structures and reach the nano-aperture at each apex. All the steps were done in presence of two dummy wafers to check the etch rates, especially annealed nitride after the LOCOS step, which normally drops by 30%. At the end, Si was etched for 10 min in a TMAH solution (25wt%, 75°C).

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Part II

Process Flows

A-1 Uniformity of SiN_x in V-grooves (nano dot formation by hot H_3PO_4)

Step	Process		Comment
1	**Substrate- Silicon <100> OSP** (#subs101)	NL-CLR-Wafer Storage Cupboard Orientation: <100> Diameter: 100mm Thickness: 525µm +/- 25µm Polished: Single side (OSP) Resistivity: 5-10Ωcm Type: p	nr. wafers: 2 nr. dummies: 4
2	**Clean HNO_3-1** (#clean102)	NL-CLR-WB14 • beaker 1: HNO_3 (99%) 5min	
3	**Clean HNO_3-2** (#clean138)	NL-CLR-WB14 • beaker 2 : HNO_3 (99%) 5min	
4	**Quick Dump Rinse (QDR)** (#clean119)	NL-CLR-Wet benches Recipe 1 QDR: 2 cycles of steps 1 till 3, 1- fill bath 5 sec 2- spray dump 15 sec 3- spray-fill 90 sec 4- end fill 200 sec Recipe 2 cascade rinsing: continuous flow Rinse till the DI resistivity is > 10 ΩM	
5	**Clean HNO_3-3a/b** (#clean 118)	NL-CR-WB14 beaker 3a/b: HNO_3 (69%), • temp 95°C, • time > 10min	
6	**Quick Dump Rinse (QDR)** (#clean119)	NL-CLR-Wet benches Recipe 1 QDR: 2 cycles of steps 1 till 3, 1- fill bath 5 sec 2- spray dump 15 sec 3- spray-fill 90 sec 4- end fill 200 sec Recipe 2 cascade rinsing: continuous flow Rinse till the DI resistivity is > 10 ΩM	
7	**Etching in HF 1% (metal free)** (#etch127)	NL-CLR-WB15 use beaker HF 1% • time variable • native oxide strip: > 1 min or hydrofobic surface etch rate: TEOS H_3 (new): 28 nm.min^{-1} Si_3N_4 H_2 (new): 0.33 nm.min^{-1}	nom. etch time: 1 min
8	**Quick Dump Rinse (QDR)** (#clean119)	NL-CLR-Wet benches Recipe 1 QDR: 2 cycles of steps 1 till 3, 1- fill bath 5 sec 2- spray dump 15 sec 3- spray-fill 90 sec 4- end fill 200 sec Recipe 2 cascade rinsing: continuous flow Rinse till the DI resistivity is > 10 ΩM	
9	**Wet oxidation of silicon @ 900°C** (#film115)	Nl-CLR- Furnace B_2 • Standby temperature: 800°C • Check water level of bubbler	nom. oxidation time: 75min layer thickness: 200nm

		• Program: WET900 • Temp.: 900°C • Gas: $H_2O + N_2$ (Bubbler)	nr. wafers: 2 nr. dummies: 2
10	**Ellipsometer measurement** (#metro107)	NL-CLR-Plasmos Ellipsometer	
11	**Lithography - Olin 907-17** (#lith057)	CR112B / Suss Micro Tech Spinner (Delta 20) Hotplate 120 °C: • Dehydration bake (120°C): 5min HexaMethylDiSilazane (HMDS): • Spin program: 4 (4000rpm, 20sec) Olin 907-17: • Spin program: 4 (4000rpm, 20sec) Hotplate 95 °C: • Prebake (95°C): 90s CR117B / EVG 620 Electronic Vision Group 620 Mask Aligner: • Hg-lamp: 12 $mW.cm^{-2}$ • Exposure Time: 4sec CR112B / Wet-Bench 11 Hotplate 120°C (CR112B or CR117B): • After Exposure Bake (120°C): 60sec Developer OPD4262: • Time: 30sec in Beaker 1 • Time: 15-30sec in Beaker 2 • Quick Dump Rinse <0.1µS • Spin drying	from front side
12	**Priming (liquid)** (#lith101)	NL-CLR-WB21/22 Primer: HexaMethylDiSilazane (HMDS) use spincoater: • program: 4000 (4000rpm, 30sec)	from back side
13	**Coating Olin Oir 907-17** (#lith105)	NL-CLR-WB21 Coating: Primus spinner • olin oir 907-17 • spin Program: 4000 (4000rpm, 30sec) Prebake: hotplate • time 90 sec • temp 95 °C	from back side
14	**Postbake Olin OiR resist** (#lith109)	NL-CLR-WB21 postbake: Hotplate • temp 120°C • time 10min	
15	**Ozone treatment of OiR resist** (#lith138)	NL-CLR/ UV PRS-100 To improve wetting of : • of chromium and oxide layers • time: 300sec	just before BHF etching
16	**Etching in BHF (1:7) metal free** (#etch124)	NL-CLR-WB15 Use dedicated beaker BHF (1:7) • temp.: 20°C. Etch rates:	nom. etch time: 3min layer thickness: 200nm

		Thermal SiO_2: 60-80 nm.min^{-1} PECVD SiO_2 : 125 nm.min^{-1} TEOS-old SiO_2: 180 nm.min^{-1} TEOS H_3 (new): 242 nm.min^{-1} Si3N4-H_2: 0.64 nm.min^{-1}	Check hydrophobicity
17	**Stripping of Olin PR - HNO_3-0** (#lith116)	NL-CLR-WB14 • Beaker 0: HNO3 (99%) • Time: 20 min or 100% removal of PR	
18	**Etching in HF 1% (metal free)** (#etch127)	NL-CLR-WB15 use beaker HF 1% • time variable • native oxide strip: > 1 min or hydrofobic surface etchrate: TEOS H_3 (new): 28 nm.min^{-1} Si3N4 H_2 (new): 0.33 nm.min^{-1}	important to do just before etching by KOH
19	**Etching in KOH standard** (#etch138)	NL-CLR-WB17 use dedicated beaker 1 or 2 • 25wt% KOH (standard recipe) • temp.: 75°C • use stirrer Etchrates: Si <100>: 1µm.min^{-1} Si <111>: 12.5 nm.min^{-1} SiO_2 (thermal): 180 nm.hr^{-1} SiRN < 0.6 nm.hr^{-1} (LPCVD ??)	nom. etch time: 20min nom. etch depth: 14.124 µm
20	**Cleaning RCA 2 private use** (#clean007)	NL-CLR-WB-09 HCL:H_2O_2:H_2O (1:1:5) vol% • add HCL to H_2O • add H_2O_2 when mixure at 70°C • temperature 70-80°C • cleaning time 10-15min • Quick Dump Rinse > 10.5 ΩM • Spin drying	time: 15min
21	**Clean HNO_3-1** (#clean102)	NL-CLR-WB14 • beaker 1: HNO_3 (99%) 5min	
22	**Clean HNO_3-2** (#clean138)	NL-CLR-WB14 • beaker 2 : HNO_3 (99%) 5min	
23	**Quick Dump Rinse (QDR)** (#clean119)	NL-CLR-Wet benches Recipe 1 QDR: 2 cycles of steps 1 till 3, 1- fill bath 5 sec 2- spray dump 15 sec 3- spray-fill 90 sec 4- end fill 200 sec Recipe 2 cascade rinsing: continuous flow Rinse till the DI resistivity is > 10 ΩM	
24	**Clean HNO_3-3a/b** (#clean 118)	NL-CR-WB14 beaker 3a/b: HNO_3 (69%), • temp 95°C, • time > 10min	
25	**Quick Dump Rinse (QDR)**	NL-CLR-Wet benches Recipe 1 QDR: 2 cycles of steps 1 till 3,	

	(#clean119)	1- fill bath 5 sec 2- spray dump 15 sec 3- spray-fill 90 sec 4- end fill 200 sec Recipe 2 cascade rinsing: continuous flow Rinse till the DI resistivity is > 10 ΩM	
26	**Etching in HF 50%** (#etch029)	NL-CLR-WB15 • use dedicated beaker: HF 50% metal free • Quick Dump Rinse <0.1µS • Spin drying Etchrate SiRN-$G_3^{\#}$: 3.1 - 3.5 nm.min^{-1} # SiRN-G_3 deposited in Nanolab Etchrate SiO_2 : 1 µm.min^{-1}	just before LPCVD nom. etch time: 2min check hydrophobicity
27	**LPCVD of SiRN (200-300 Mpa)** (#film155)	NL-CLR-Tempress LPCVD G_4 CONTACT: ITE-JAN FOR STATUS OF G4 Program: XXXX • SiH_2Cl_2 flow: 150sccm • NH_3 flow: 50 sccm • temperature: 830/850/870°C • pressure: 200 mTorr • deposition rate: ± 6,6 nm.min^{-1} ?? • N_f: ± 2.18 ??? • Stress (range): 200-280 Mpa. ??	layer tichness: 250nm program: ? nom. deposition rate: 10.00 nm.min-1 nom. deposition time: 25 min nr. wafers: 2 nr. dummies: 2
28	**Ellipsometer measurement** (#metro107)	NL-CLR-Plasmos Ellipsometer	
29			HRSEM
30	**Etching in (hot) H_3PO_4** (#etch153)	NL-CLR-WB08 Use dedicated beaker with reflux lid for etching	temperature: 180 ^{0}C etch factor: 0.40t, 0.60t, 1.00t, 1.23t, 1.35t and 1.50t nom. etch rate: 3.83 nm.min-1

Table 1 : Etch rates values old Cleanroom (without reflux and without lid!)

Temperature [°C]	Er SiRN-G_3 [nm.min^{-1}]	Er SiO_2 A_2 [nm.min^{-1}]
180	4.1	0.48
160	1.4	0.16
140	0.5	0.05

Table 2: Etch rate values fresh prepared H3PO4 in new CR by Yiping (with lid and without lid cooling)

Temperature [°C]	Er SiRN-G_3 [nm.min^{-1}]	Er SiO_2 [nm.min^{-1}]
180	6.1-6.6	0.6
160	2.35	0.18
140		

Table 3: Etch rate values after 50 days in new Cleanroom by Erwin (with lid and without lid cooling)

Temperature [°C]	Er SiRN-G_3 [nm.min^{-1}]	Er SiO_2 800°C [nm.min^{-1}]
180	4.5	0.47
160		

Table 4: Si3N4 LPCVD-H2 by Christiaan, Etchrate values after 50 days in new Cleanroom

Temperature [°C]	Er Si3N4 -H2 [nm.min^{-1}]	
180	4,7	
160	1,8	

31	**Ellipsometer measurement** (#metro107)	NL-CLR-Plasmos Ellipsometer	
32			HRSEM for all samples after etching is necessary

A-2 Uniformity of SiN_x in V-grooves (nano dot formation by HF 50%)

Step	Process		Comment
1	**Substrate- Silicon <100> OSP** (#subs101)	NL-CLR-Wafer Storage Cupboard Orientation: <100> Diameter: 100mm Thickness: 525µm +/- 25µm Polished: Single side (OSP) Resistivity: 5-10Ωcm Type: p	nr. wafers: 2 nr. dummies: 4
2	**Clean HNO_3-1** (#clean102)	NL-CLR-WB14 • beaker 1: HNO_3 (99%) 5min	
3	**Clean HNO_3-2** (#clean138)	NL-CLR-WB14 • beaker 2 : HNO_3 (99%) 5min	
4	**Quick Dump Rinse (QDR)** (#clean119)	NL-CLR-Wet benches Recipe 1 QDR: 2 cycles of steps 1 till 3, 1- fill bath 5 sec 2- spray dump 15 sec 3- spray-fill 90 sec 4- end fill 200 sec Recipe 2 cascade rinsing: continuous flow Rinse till the DI resistivity is > 10 ΩM	
5	**Clean HNO_3-3a/b** (#clean 118)	NL-CR-WB14 beaker 3a/b: HNO_3 (69%), • temp 95°C, • time > 10min	
6	**Quick Dump Rinse (QDR)** (#clean119)	NL-CLR-Wet benches Recipe 1 QDR: 2 cycles of steps 1 till 3, 1- fill bath 5 sec 2- spray dump 15 sec 3- spray-fill 90 sec 4- end fill 200 sec Recipe 2 cascade rinsing: continuous flow Rinse till the DI resistivity is > 10 ΩM	
7	**Etching in HF 1% (metal free)** (#etch127)	NL-CLR-WB15 use beaker HF 1% • time variable • native oxide strip: > 1 min or hydrofobic surface etch rate: TEOS H_3 (new): 28 $nm.min^{-1}$ Si_3N_4 H_2 (new): 0.33 $nm.min^{-1}$	nom. etch time: 1 min
8	**Quick Dump Rinse (QDR)** (#clean119)	NL-CLR-Wet benches Recipe 1 QDR: 2 cycles of steps 1 till 3, 1- fill bath 5 sec 2- spray dump 15 sec 3- spray-fill 90 sec 4- end fill 200 sec Recipe 2 cascade rinsing: continuous flow Rinse till the DI resistivity is > 10 ΩM	
9	**Wet oxidation of silicon @ 900°C** (#film115)	Nl-CLR- Furnace B_2 • Standby temperature: 800°C • Check water level of bubbler	nom. oxidation time: 75min layer thickness: 200nm

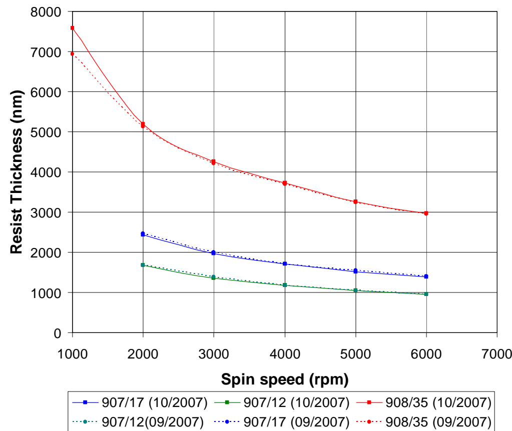
		• Program: WET900 • Temp.: 900°C • Gas: $H_2O + N_2$ (Bubbler)	nr. wafers: 2 nr. dummies: 2
10	**Ellipsometer measurement** (#metro107)	NL-CLR-Plasmos Ellipsometer	
11	**Lithography - Olin 907-17** (#lith057)	CR112B / Suss Micro Tech Spinner (Delta 20) Hotplate 120 °C: • Dehydration bake (120°C): 5min HexaMethylDiSilazane (HMDS): • Spin program: 4 (4000rpm, 20sec) Olin 907-17: • Spin program: 4 (4000rpm, 20sec) Hotplate 95 °C: • Prebake (95°C): 90s CR117B / EVG 620 Electronic Vision Group 620 Mask Aligner: • Hg-lamp: 12 $mW.cm^{-2}$ • Exposure Time: 4sec CR112B / Wet-Bench 11 Hotplate 120°C (CR112B or CR117B): • After Exposure Bake (120°C): 60sec Developer OPD4262: • Time: 30sec in Beaker 1 • Time: 15-30sec in Beaker 2 • Quick Dump Rinse <0.1µS • Spin drying	from front side
12	**Priming (liquid)** (#lith101)	NL-CLR-WB21/22 Primer: HexaMethylDiSilazane (HMDS) use spincoater: • program: 4000 (4000rpm, 30sec)	from back side
13	**Coating Olin Oir 907-17** (#lith105)	NL-CLR-WB21 Coating: Primus spinner • olin oir 907-17 • spin Program: 4000 (4000rpm, 30sec) Prebake: hotplate • time 90 sec • temp 95 °C	from back side
14	**Postbake Olin OiR resist** (#lith109)	NL-CLR-WB21 postbake: Hotplate • temp 120°C • time 10min	
15	**Ozone treatment of OiR resist** (#lith138)	NL-CLR/ UV PRS-100 To improve wetting of : • of chromium and oxide layers • time: 300sec	just before BHF etching
16	**Etching in BHF (1:7) metal free** (#etch124)	NL-CLR-WB15 Use dedicated beaker BHF (1:7) • temp.: 20°C. Etch rates:	nom. etch time: 3min layer thickness: 200nm Check

		Thermal SiO_2: 60-80 $nm.min^{-1}$ PECVD SiO_2 : 125 $nm.min^{-1}$ TEOS-old SiO_2: 180 $nm.min^{-1}$ TEOS H_3 (new): 242 $nm.min^{-1}$ Si3N4-H_2: 0.64 $nm.min^{-1}$	hydrophobicity
17	**Stripping of Olin PR - HNO_3-0** (#lith116)	NL-CLR-WB14 • Beaker 0: HNO3 (99%) • Time: 20 min or 100% removal of PR	
18	**Etching in HF 1% (metal free)** (#etch127)	NL-CLR-WB15 use beaker HF 1% • time variable • native oxide strip: > 1 min or hydrofobic surface etchrate: TEOS H_3 (new): 28 $nm.min^{-1}$ Si3N4 H_2 (new): 0.33 $nm.min^{-1}$	important to do just before etching by KOH
19	**Etching in KOH standard** (#etch138)	NL-CLR-WB17 use dedicated beaker 1 or 2 • 25wt% KOH (standard recipe) • temp.: 75°C • use stirrer Etchrates: Si <100>: 1$\mu m.min^{-1}$ Si <111>: 12.5 $nm.min^{-1}$ SiO_2 (thermal): 180 $nm.hr^{-1}$ SiRN < 0.6 $nm.hr^{-1}$ (LPCVD ??)	nom. etch time: 20min nom. etch depth: 14.124 µm
20	**Cleaning RCA 2 private use** (#clean007)	NL-CLR-WB-09 HCL:H_2O_2:H_2O (1:1:5) vol% • add HCL to H_2O • add H_2O_2 when mixure at 70°C • temperature 70-80°C • cleaning time 10-15min • Quick Dump Rinse > 10.5 ΩM • Spin drying	time: 15min
21	**Clean HNO_3-1** (#clean102)	NL-CLR-WB14 • beaker 1: HNO_3 (99%) 5min	
22	**Clean HNO_3-2** (#clean138)	NL-CLR-WB14 • beaker 2 : HNO_3 (99%) 5min	
23	**Quick Dump Rinse (QDR)** (#clean119)	NL-CLR-Wet benches Recipe 1 QDR: 2 cycles of steps 1 till 3, 1- fill bath 5 sec 2- spray dump 15 sec 3- spray-fill 90 sec 4- end fill 200 sec Recipe 2 cascade rinsing: continuous flow Rinse till the DI resistivity is > 10 ΩM	
24	**Clean HNO_3-3a/b** (#clean 118)	NL-CR-WB14 beaker 3a/b: HNO_3 (69%), • temp 95°C, • time > 10min	
25	**Quick Dump Rinse (QDR)**	NL-CLR-Wet benches Recipe 1 QDR: 2 cycles of steps 1 till 3,	

	(#clean119)	1- fill bath 5 sec 2- spray dump 15 sec 3- spray-fill 90 sec 4- end fill 200 sec Recipe 2 cascade rinsing: continuous flow Rinse till the DI resistivity is > 10 ΩM	
26	**Etching in HF 50%** (#etch029)	NL-CLR-WB15 • use dedicated beaker: HF 50% metal free • Quick Dump Rinse <0.1µS • Spin drying Etchrate SiRN-G_3#: 3.1 - 3.5 $nm.min^{-1}$ # SiRN-G_3 deposited in Nanolab Etchrate SiO_2 : 1 $\mu m.min^{-1}$	just before LPCVD nom. etch time: 2min check hydrophobicity
27	**LPCVD of SiRN (200-300 Mpa)** (#film155)	NL-CLR-Tempress LPCVD G_4 CONTACT: ITE-JAN FOR STATUS OF G4 Program: XXXX • SiH_2Cl_2 flow: 150sccm • NH_3 flow: 50 sccm • temperature: 830/850/870°C • pressure: 200 mTorr • deposition rate: ± 6,6 $nm.min^{-1}$?? • N_f: ± 2.18 ??? • Stress (range): 200-280 Mpa. ??	layer tichness: 250nm program: ? nom. deposition rate: 10.00 nm.min-1 nom. deposition time: 25 min nr. wafers: 2 nr. dummies: 2
28	**Ellipsometer measurement** (#metro107)	NL-CLR-Plasmos Ellipsometer	
29			HRSEM
30	**Etching in HF 50% (metal free)** (#etch129)	NL-CLR-WB15 use dedicated beaker: HF 50% metal free • temp.: 20 °C etchrate • SiRN-G3# (nanolab): 3.1 - 3.5 $nm.min^{-1}$ • SiO_2: 1 $\mu m.min^{-1}$ • Si_3N_4-H_2: 11.6 $nm.min^{-1}$	temperature: 180C Etch factor: 0.40t, 0.60t, 1.00t, 1.23t, 1.35t and 1.50t nom. etch rate: 3.83 nm.min-1
31	**Ellipsometer measurement** (#metro107)	NL-CLR-Plasmos Ellipsometer	
32			HRSEM for all samples after etching is necessary

A-3 Batch fabricated thermal/Hall Sensor on the AFM tip

<table>
<tr><th>Step</th><th>Process</th><th></th><th>Comment</th></tr>
<tr><td>1</td><td>Substrate Selection
Silicon Wafer</td><td>Diameter: 4 ’’
Thickness: 380 µm (± 25)
Crystallographic Orientation: (100)
Doping: (n-type)
Resistivity: 1 – 10 Ωcm
Polishing: OSP</td><td>nr. wafers: 4</td></tr>
<tr><td>2</td><td>Wafer Cleaning
Nitric Acid
(HNO_3)</td><td>CR112B / Wet-Bench 3-2
Removal of organic (100 % HNO_3) and metallic (69% HNO_3) contamination.
Chemicals:
HNO_3 (100%) Selectipur: MERCK 100453
HNO_3 (69%) VLSI: MERCK 116445
Procedure:
• Beaker 1: fumic HNO_3 (100%), 5min
• Beaker 2: fumic HNO_3 (100%), 5min
• Quick Dump Rinse <0.1µS
• Beaker 3: boiling (95°C) HNO_3 (69%), 10min
• Quick Dump Rinse <0.1µS
• Spin drying
Remarks:
No metal on the wafers!</td><td></td></tr>
<tr><td>3</td><td>Surface Cleaning
Oxide Strip
HF (1%)</td><td>CR112B / Wet-Bench 3-3
Chemicals:
HF (1%) VLSI: MERCK 112629.500
Procedure:
• Beaker 1: HF (1%), >1min
• Quick Dump Rinse <0.1µS
• Spin drying</td><td></td></tr>
<tr><td>4</td><td>Deposition
CVD
LPCVD
(Silicon Nitride)
Low Stress</td><td>CR125C / Tempress LPCVD/HC
Tube:
Program:
LPCVD deposition of low stress silicon rich nitride (Si_RN).
Process conditions:
• SiH2Cl2 flow: 70sccm
• NH3 flow: 18sccm
• Temperature: 850°C
• Pressure: 200mTorr
• Deposition rate: 3.85 $nm.min^{-1}$</td><td>nom. deposition time: 1hr 30min
layer thickness: 346 nm</td></tr>
<tr><td>5</td><td>Optical Lithography
Resist Coating
Automatic Coater
Positive resist
(907-12, -17, -35)</td><td>CR 117B
Resist coater – SSE Maximus 804
Chemicals: 907-12, 907-17 and 907-35
Procedure:</td><td>resist: 907-12
HMDS: Yes (vapor deposition)
rpm: 4000
EBR: No</td></tr>
</table>



6	**Optical Lithography Exposure EVG 620 Manual Positive resist (907-12, -17, -35)**	CR 117B EVG 620 mask aligner with manual control. RPM | 907-12 | 907-12 | 907-12 1000 2000 3000 4000 | 3sec 5000 Remarks: *For a proper vacuum contact the pressure should be around 0.8 !*	mode: Vacuum Contact resist: 907-12 time: 3.0 sec mask: Hall Sensor 1
7	**Optical Lithography Development Positive resist (907-12, -17, -35)**	CR112B / Wet-Bench 11 Chemicals: OPD4262 Procedure: • Soak wafers for 30s in Beaker 1; • Soak wafers for 15s-30s in Beaker 2; • Quick Dump Rinse <0.1µS • Spin drying Remarks: *Move the wafers slowly during the development!*	beaker 1: 30sec beaker 2: 20sec
8	**Etching RIE (Silicon Nitride)**	CR102A Elektrotech PF310/340 (Etske) *Plasma etching of silicon nitride.* • Electrode Temperature: 10 °C • Dirty chamber; • Quartz electrode Pressure 25 Pa CHF_3 flow 50 sccm O_2 flow 5 sccm RF power 75 W Etch rates: Silicon nitride: 50 $nm.min^{-1}$ (for VDC: -460V) Photoresist (Olin): 95 $nm.min^{-1}$	layer: SiRN layer thickness: 350 nm mask: Photoresist 917/12 nom. etch time: 8min DC Bias: ~400 V

		Remarks: *If DC-Bias < 375 V clean the chamber wit O_2 plasma!*	
9	**Surface Cleaning Plasma Ashing (O_2 plasma)**	CR125C/ Ozone Reactor UV PRS-100 *Removal of organic contamination with ozone at atmospheric condition (resist stripping).* Process parameters O_2 flow 50 sccm RF power 500 W Remarks: *Process used to remove resist.*	nom. etch time: 10min
10	**Resist stripping Nitric Acid (HNO_3 100%)**	CR112B / Wet-Bench 3-2 *Resist removal with 100 % nitric acid (HNO_3)!* Chemicals: HNO_3 (100%) Selectipur: MERCK 100453 Procedure: • Beaker 1: fumic HNO3 (100%), 5min • Quick Dump Rinse <0.1µS • Spin drying Remarks: *No metal on the wafers!*	nom. etch time: 10min
11	**Wafer Cleaning Nitric Acid (HNO_3)**	CR112B / Wet-Bench 3-2 *Removal of organic (100 % HNO_3) and metallic (69% HNO_3) contamination.* Chemicals: HNO_3 (100%) Selectipur: MERCK 100453 HNO_3 (69%) VLSI: MERCK 116445 Procedure: • Beaker 1: fumic HNO_3 (100%), 5min • Beaker 2: fumic HNO_3 (100%), 5min • Quick Dump Rinse <0.1µS • Beaker 3: boiling (95°C) HNO3 (69%), 10min • Quick Dump Rinse <0.1µS • Spin drying Remarks: *No metal on the wafers!*	
12	**Deposition CVD LPCVD (Silicon Oxide) TEOS**	CR112B / Tempress LPCVD Tube: B4 -TEOS Program: $TEOS_{02}$ *LPCVD deposition ofsilicon oxide from TEOS ($Si(OC_2H_5)_4$).* Process conditions: • Temperature: 700 °C • Pressure: 400 mTorr • Bubbler: 40.0 °C • Deposition rate: 10.2 $nm.min^{-1}$ CR112B / Tempress LPCVD	nom. Deposition time: 20 min layer thickness: 200 nm
13	**Annealing 1100°C**	CR112B / Furnace B_3 Program: ANN1100C *Annealing at 1100°C with N2 for diffusion of B or P and annealing for Silicon-Silicon bonding.* • Temperature: 1100°C	nom. annealing time: 2hrs

- Gas: N2
- Flow: 1 $l.min^{-1}$
- Ramp: 20 $°C.min^{-1}$

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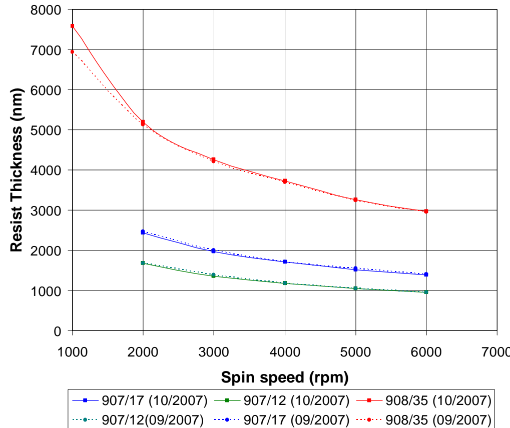
14 — Optical Lithography / Resist Coating / Automatic Coater / Positive resist (907-12, -17, -35)

CR 117B
Resist coater – SSE Maximus 804
Chemicals: 907-12, 907-17 and 907-35
Procedure:



resist: 907-12
HMDS: Yes (vapor deposition)
rpm: 4000
EBR: No

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15 — Optical Lithography / Exposure / EVG 620 Manual / Positive resist (907-12, -17, -35)

CR 117B
EVG 620 mask aligner with manual control.

RPM	907-12	907-12	907-12
1000			
2000			
3000			
4000	3sec		
5000			

Remarks:
For a proper vacuum contact the pressure should be around 0.9 !

mode: Vacuum Contact
resist: 907-12
time: 3.5 sec
mask: Hall sensor 2

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16 — Optical Lithography / Development / Positive resist (907-12, -17, -35)

CR112B / Wet-Bench 11
Chemicals: OPD4262
Procedure:
- Soak wafers for 30s in Beaker 1;
- Soak wafers for 15s-30s in Beaker 2;
- Quick Dump Rinse <0.1µS
- Spin drying

Remarks:
Move the wafers slowly during the development!

beaker 1: 30sec
beaker 2: 20sec

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17 — Optical Lithography / Post-bake / Positive resist (907-12, -17, -35)

CR112B / Hotplate
- Temperature: 120 °C
- Time: 1 min

Remarks:
Long baking time (30m -40m) when the resist is used as a mask for BHF etching.

temperature: 120 °C
time: 40min

---

18 — Etching / Wet Chemical

CR116B / Wet-Bench 2
Etching of silicon oxide.

nom. etch time: 3min
layer: TEOS (200 nm) Annealed!

	Etching **(BHF)**	Chemicals: NH4F/HF (1:7) VLSI: MERCK 101171.2500 Procedure: • BHF (T: 20 ^{o}C) • Quick Dump Rinse <0.1µS • Spin drying Etch rates: Thermal SiO_2: 60-80nm.min^{-1} TEOS SiO_2: 180 nm.min^{-1} PECVD SiO_2: 125 nm.min^{-1}	
19	**Etching** **RIE** **(Silicon Nitride)**	CR102A Elektrotech PF310/340 (Etske) *Plasma etching of silicon nitride.* • Electrode Temperature: 10 ^{o}C • Dirty chamber; • Quartz electrode Pressure 25 Pa CHF_3 flow 50 sccm O_2 flow 5 sccm RF power 75 W Etch rates: Silicon nitride: 50 nm.min^{-1} (for VDC: -460V) Photoresist (Olin): 95 nm.min^{-1} Remarks: *If DC-Bias < 375 V clean the chamber wit O_2 plasma!*	layer: SiRN layer thickness: 100 nm mask: Photoresist 917/12 time: 8min
20	**Surface Cleaning** **Plasma Ashing** **(O2 plasma)**	CR125C/ Ozone Reactor UV PRS-100 *Removal of organic contamination with ozone at atmospheric condition (resist stripping).* Process parameters O_2 flow 50 sccm RF power 500 W Remarks: *Process used to remove resist.*	nom. etch time: 10min
21	**Resist stripping** **Nitric Acid** **(HNO_3 100%)**	CR112B / Wet-Bench 3-2 *Resist removal with 100 % nitric acid (HNO_3)!* Chemicals: HNO3 (100%) Selectipur: MERCK 100453 Procedure: • Beaker 1: fumic HNO3 (100%), 5min • Quick Dump Rinse <0.1µS • Spin drying Remarks: *No metal on the wafers!*	time: 10min
22	**Etching** **Wet Chemical** **Etching** **(KOH 25wt%)**	CR102B / KOH Anisotropic etching of silicon! Chemicals: KOH: MERCK 105019.500 Ratio: • KOH:DI (1:3)	nom. etch time:10min

		(500g KOH pellets in 1500ml DI water) Procedure: • Temp.: 75°C • Stirrer on • Quick Dump Rinse <0.1µS • Spin drying Etch rates: Si <100>: 1µm.min^{-1} Si <111>: 12.5nm.min^{-1} SiO_2 (thermal): 180nm.hr^{-1} SiRN: < 0.6nm.hr^{-1} Remarks: *After etching the wafers should be cleaned using RCA-2 Process (HCl/H2O2/H2O)!*	
23	**Surface Cleaning** **RCA-2 Process** **($HCl/H_2O_2/H_2O$)**	Hot plate (3F & 1F) *Desorbs residual metals and dissolves alkali ions and hydroxides of Al_3^+, Mg_3^+, Fe_3^+.* Chemicals: HCl(30%): xxxxxx H_2O_2 (30%) Kanto Chemical Co. Inc H_2O (DI water) • Ratio: HCl(30%): H_2O_2(30%): H_2O (1:1:5) • Temperature: 80 °C • Cleaning Time: 5 – 10 min Procedure: • Add HCl to H_2O • Heat the solution at the hot plate. • Add H_2O_2 to solution at 70 °C! • Put wafers in the solution at 80 °C Rinsing with DI water!	time:10min
24	**Wafer Cleaning** **Nitric Acid** **(HNO_3)**	CR112B / Wet-Bench 3-2 *Removal of organic (100 % HNO_3) and metallic (69% HNO_3) contamination.* Chemicals: HNO_3 (100%) Selectipur: MERCK 100453 HNO_3 (69%) VLSI: MERCK 116445 Procedure: • Beaker 1: fumic HNO_3 (100%), 5min • Beaker 2: fumic HNO_3 (100%), 5min • Quick Dump Rinse <0.1µS • Beaker 3: boiling (95°C) HNO3 (69%), 10min • Quick Dump Rinse <0.1µS • Spin drying Remarks: *No metal on the wafers!*	
25	**Etching** **Wet Chemical** **Etching** **(BHF)**	CR116B / Wet-Bench 2 *Etching of silicon oxide.* Chemicals: NH4F/HF (1:7) VLSI: MERCK 101171.2500 Procedure: • BHF (T: 20°C) • Quick Dump Rinse <0.1µS • Spin drying	nom. etch time: 4min

		Etch rates: Thermal SiO_2: 60-80nm.min^{-1} TEOS SiO_2: 180 nm.min^{-1} PECVD SiO_2: 125 nm.min^{-1}	
26	**Deposition** **CVD** **LPCVD** **(Silicon Nitride)** **Low Stress**	CR125C / Tempress LPCVD/HC Tube: G3 (LPCVD SiRN) Program: N2(SIRN01) *LPCVD deposition of low stress silicon rich nitride (Si_RN).* Process conditions: • SiH2Cl2 flow: 70sccm • NH3 flow: 18sccm • Temperature: 850°C • Pressure: 200mTorr • Deposition rate: 3.85 nm.min^{-1}	nom. deposition time: 50min layer thickness: 192 nm
27	**Etching** **Wet Chemical** **Etching** **(HF 50%)**	CR112B / Wet-Bench 3-3 *Etching of silicon oxide or silicon nitride.* Chemicals: HF (50%) VLSI: MERCK 100373.2500 Procedure: • HF 50% (T: 20 °C) • Quick Dump Rinse <0.1µS • Spin drying • Quick Dump Rinse <0.1µS Etch rates: SiO2: 1 µm.min^{-1} LPCVD Si_RN: 3 – 5 nm.min^{-1}	nom. etch time: 80 min
28	**Deposition** **CVD** **LPCVD** **(Silicon Oxide)** **TEOS**	CR112B / Tempress LPCVD Tube: B4 -TEOS Program: $TEOS_{02}$ *LPCVD deposition ofsilicon oxide from TEOS ($Si(OC_2H_5)_4$).* Process conditions: • Temperature: 700 °C • Pressure: 400 mTorr • Bubbler: 40.0 °C • Deposition rate: 10.2 nm.min^{-1} CR112B / Tempress LPCVD	nom. deposition time: 40min layer thickness: 400 nm
29	**Annealing** **1100°C**	CR112B / Furnace B3 Program: ANN1100C *Annealing at 1100°C with N2 for diffusion of B or P and annealing for Silicon-Silicon bonding.* • Temperature: 1100°C • Gas: N2 • Flow: 1 l.min^{-1} • Ramp: 20 °C.min^{-1}	nom. annealing time: 2hrs
30	**Deposition** **CVD** **LPCVD** **(Silicon Nitride)** **Low Stress**	CR125C / Tempress LPCVD/HC Tube: G_3 (LPCVD SiRN) Program: $N_2(SIRN_{01})$ *LPCVD deposition of low stress silicon rich nitride (Si_RN).* Process conditions: • SiH_2Cl_2 flow: 70sccm • NH_3 flow: 18sccm	nom. deposition time: 1hr 30min layer thickness: 350 nm

<table>
<tr><td></td><td></td><td>• Temperature: 850°C
• Pressure: 200mTorr
• Deposition rate: 3.85 nm.min^{-1}</td><td></td></tr>
<tr><td>31</td><td>Deposition
CVD
LPCVD
(Silicon Oxide)
TEOS</td><td>CR112B / Tempress LPCVD
Tube: B4 -TEOS
Program: TEOS$_{02}$
LPCVD deposition ofsilicon oxide from TEOS ($Si(OC_2H_5)_4$).
Process conditions:
• Temperature: 700 °C
• Pressure: 400 mTorr
• Bubbler: 40.0 °C
• Deposition rate: 10.2 nm.min^{-1}
CR112B / Tempress LPCVD</td><td>nom. deposition time: 11min
layer thickness: 110 nm</td></tr>
<tr><td>32</td><td>Annealing
1100°C</td><td>CR112B / Furnace B3
Program: ANN1100C
Annealing at 1100°C with N_2 for diffusion of B or P and annealing for Silicon-Silicon bonding.
• Temperature: 1100°C
• Gas: N_2
• Flow: 1 l.min^{-1}
• Ramp: 20 °C.min^{-1}</td><td>nom. annealing time: 2hrs</td></tr>
<tr><td>33</td><td>Optical Lithography
Resist Coating
Automatic Coater
Positive resist
(907-12, -17, -35)</td><td>CR 117B
Resist coater – SSE Maximus 804
Chemicals: 907-12, 907-17 and 907-35
Procedure:</td><td>resist: 907-35
HMDS: Yes (vapor deposition)
rpm: 4000
EBR: No</td></tr>
<tr><td>34</td><td>Optical Lithography
Exposure
EVG 620 Manual
Positive resist
(907-12, -17, -35)</td><td>CR 117B
EVG 620 mask aligner with manual control.
<table><tr><th>RPM</th><th>907-12</th><th>907-12</th><th>907-12</th></tr><tr><td>1000</td><td></td><td></td><td></td></tr><tr><td>2000</td><td></td><td></td><td></td></tr><tr><td>3000</td><td></td><td></td><td></td></tr><tr><td>4000</td><td>3sec</td><td></td><td></td></tr><tr><td>5000</td><td></td><td></td><td></td></tr></table></td><td>mode: Hard Contact
resist: 907-17
time: 8sec
mask: Hall sensor 3</td></tr>
</table>

		Remarks: *For a proper vacuum contact the pressure should be around 0.9 !*	
35	**Optical Lithography** **Development** **Positive resist** **(907-12, -17, -35)**	CR112B / Wet-Bench 11 Chemicals: OPD4262 Procedure: • Soak wafers for 30s in Beaker 1; • Soak wafers for 15s-30s in Beaker 2; • Quick Dump Rinse <0.1µS • Spin drying Remarks: *Move the wafers slowly during the development!*	beaker 1: 30sec beaker 2: 20sec
36	**Optical Lithography** **Post-bake** **Positive resist** **(907-12, -17, -35)**	CR112B / Hotplate • Temperature: 120 ^{o}C • Time: 1 min Remarks: *Long baking time (30m -40m) when the resist is used as a mask for BHF etching.*	temperature: 120 ^{o}C time: 40min
37	**Etching** **Wet Chemical Etching** **(BHF)**	CR116B / Wet-Bench 2 *Etching of silicon oxide.* Chemicals: NH4F/HF (1:7) VLSI: MERCK 101171.2500 Procedure: • BHF (T: 20 ^{o}C) • Quick Dump Rinse <0.1µS • Spin drying Etch rates: Thermal SiO_2: 60-80nm.min^{-1} TEOS SiO_2: 180 nm.min^{-1} PECVD SiO_2: 125 nm.min^{-1}	nom. etch time: 1min 30sec layer: TEOS (100 nm) Annealed!
38	**Etching** **RIE** **(Silicon Nitride)**	CR102A Elektrotech PF310/340 (Etske) *Plasma etching of silicon nitride.* • Electrode Temperature: 10 ^{o}C • Dirty chamber; • Quartz electrode Pressure 25 Pa CHF_3 flow 50 sccm O_2 flow 5 sccm RF power 75 W Etch rates: Silicon nitride: 50 nm.min^{-1} (for VDC:-460V) Photoresist (Olin): 95 nm.min^{-1} Remarks: *If DC-Bias < 375 V clean the chamber wit O_2 plasma!*	layer: SiRN layer thickness: 350 nm mask: Photoresist 917/35 time: ~8min check with a dummy wafer
39	**Surface Cleaning** **Plasma Ashing** **(O_2 plasma)**	CR125C/ Ozone Reactor UV PRS-100 *Removal of organic contamination with ozone at atmospheric condition (resist stripping).* Process parameters O_2 flow 50 sccm	nom. etch time: 5min

		RF power 500 W Remarks: *Process used to remove resist.*	
40	**Resist stripping Nitric Acid (HNO_3 100%)**	CR112B / Wet-Bench 3-2 *Resist removal with 100 % nitric acid (HNO_3)!* Chemicals: HNO_3 (100%) Selectipur: MERCK 100453 Procedure: • Beaker 1: fumic HNO_3 (100%), 5min • Quick Dump Rinse <0.1µS • Spin drying Remarks: *No metal on the wafers!*	time: 10min
41	**Wafer Cleaning Nitric Acid (HNO_3)**	CR112B / Wet-Bench 3-2 *Removal of organic (100 % HNO_3) and metallic (69% HNO_3) contamination.* Chemicals: HNO_3 (100%) Selectipur: MERCK 100453 HNO_3 (69%) VLSI: MERCK 116445 Procedure: • Beaker 1: fumic HNO_3 (100%), 5min • Beaker 2: fumic HNO_3 (100%), 5min • Quick Dump Rinse <0.1µS • Beaker 3: boiling (95°C) HNO3 (69%), 10min • Quick Dump Rinse <0.1µS • Spin drying Remarks: *No metal on the wafers!*	
42	**Wafer Cleaning Oxide Strip HF (1%)**	CR112B / Wet-Bench 3-3 Chemicals: HF (1%) VLSI: MERCK 112629.500 Procedure: • Beaker 1: HF (1%), >1min • Quick Dump Rinse <0.1µS • Spin drying	nom. etch time: 30sec
43	**Etching Wet Chemical Etching (H_3PO_4)**	CR112B / Wet-Bench 3-1 Chemicals: H_3PO_4 85% Merck VLSI 1.00568.2500 • Temp.: 180°C (caution!) • Quick Dump Rinse <0.1µS • Spin drying Etchrates: SiRN 4.1nm.min^{-1}, SiO_2 0.48nm.min^{-1} (180°C); SiRN 1.4nm.min^{-1}, SiO_2 0.16nm.min^{-1} (160°C); SiRN 0.5nm.min^{-1}, SiO_2 0.05nm.min^{-1} (140°C); Remarks: *Only SiO_2, Silicon, PolySilicon, SiRN, SiON, SiON are allowed. Apply always first a Standard Wafer Clean and a 1% HF dip to remove native oxide.*	nom. etch time: 1hr 30min temperature: 180°C nom. etch rate: 4.1 nm.min^{-1}

44	**Thermal Oxidation** **Wet oxidation** **(1000 ^oC)**	CR112B / Furnace B2 Program: WOX-1000 *Wet oxidation of silicon nitride at 1000 ^oC.* • Temperature: 1150°C • Gas: $H_2O + N_2$ (Bubbler) • Oxidation time (min) Remarks: *Check water level of bubbler before oxidation!*	nom. oxidation time: 2hrs Wafers ready for the bonding with a glass wafer!